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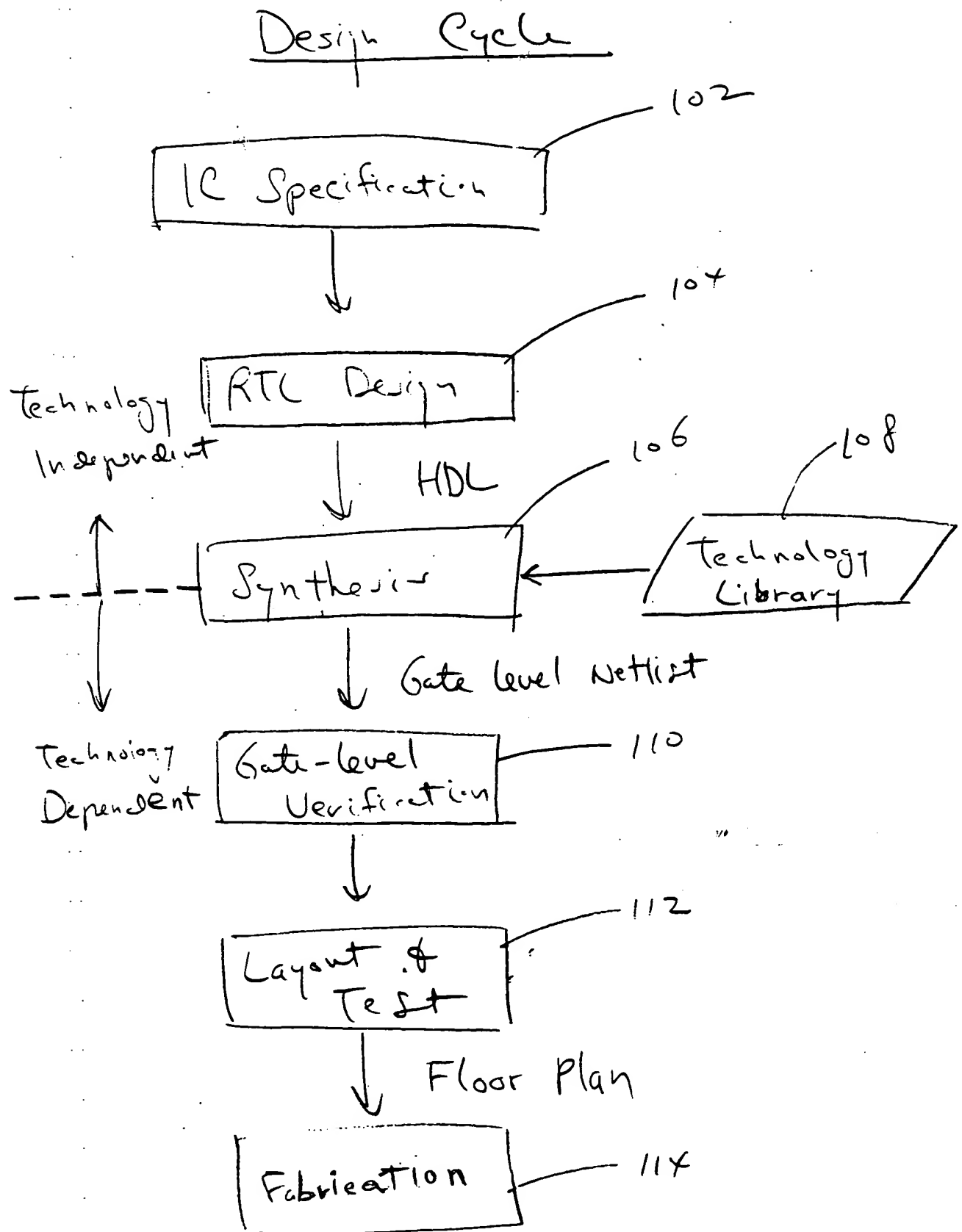
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FIGURE 1



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FIGURE 2

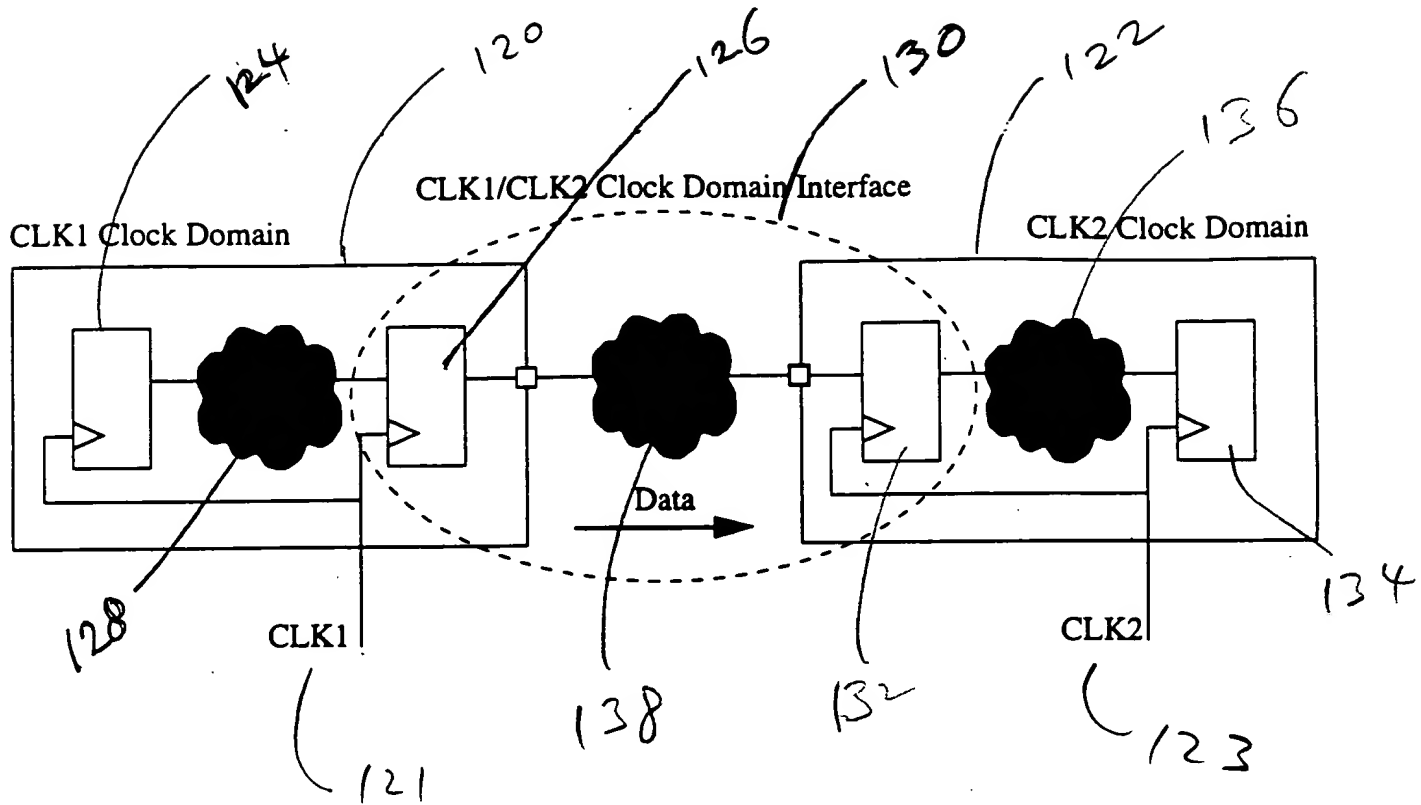


FIGURE 4

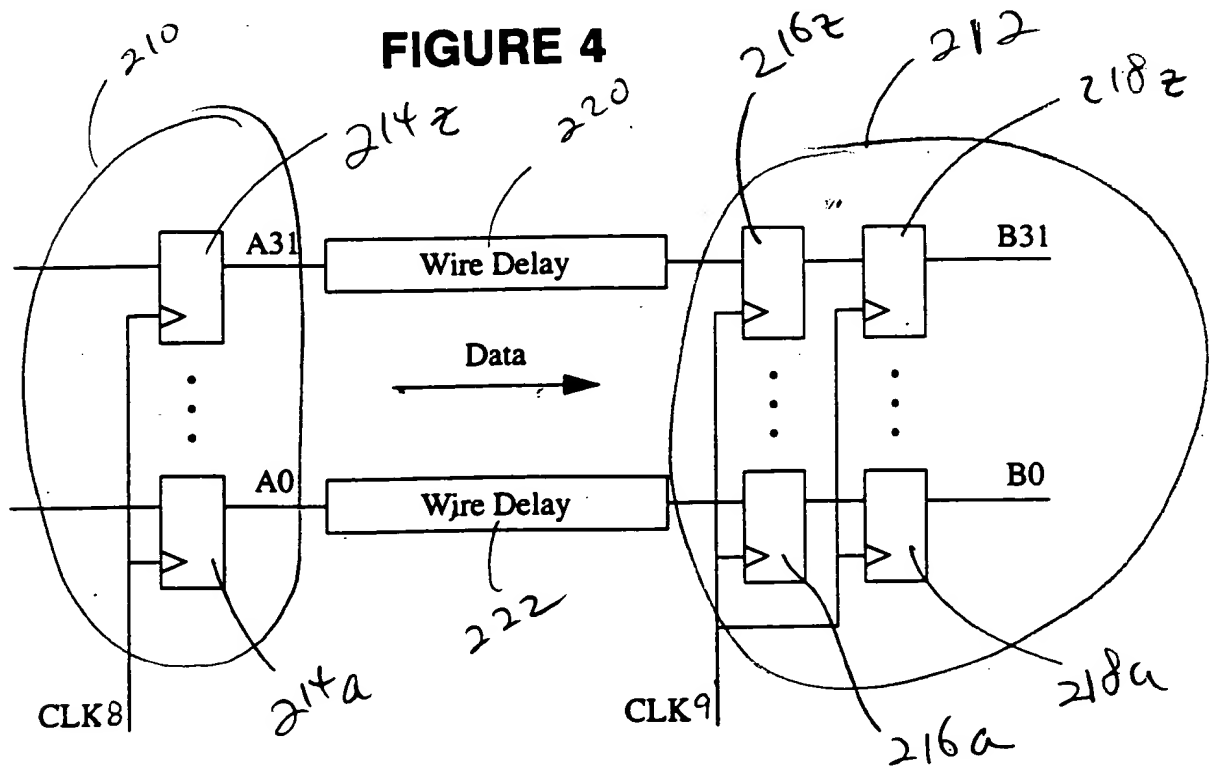


FIGURE 3A

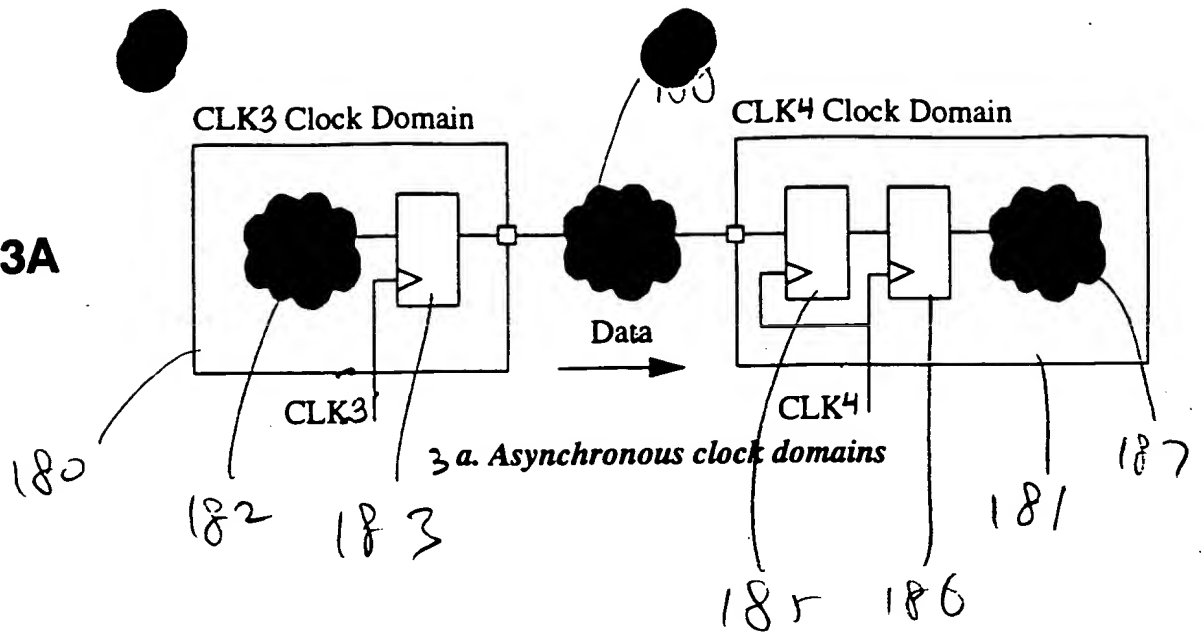


FIGURE 3B

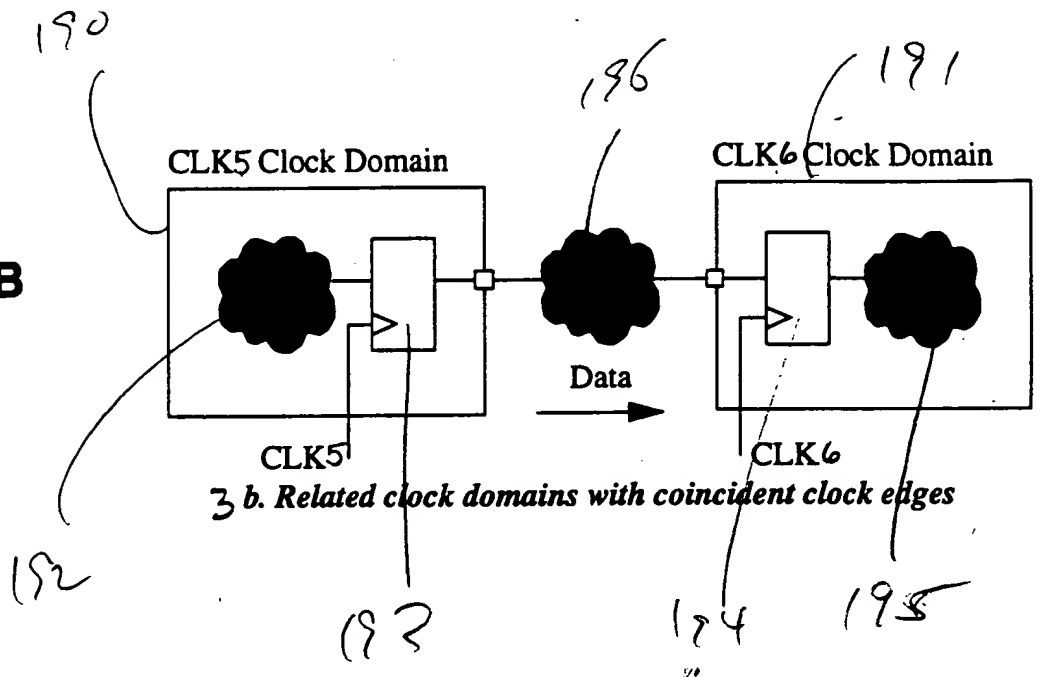


FIGURE 3C

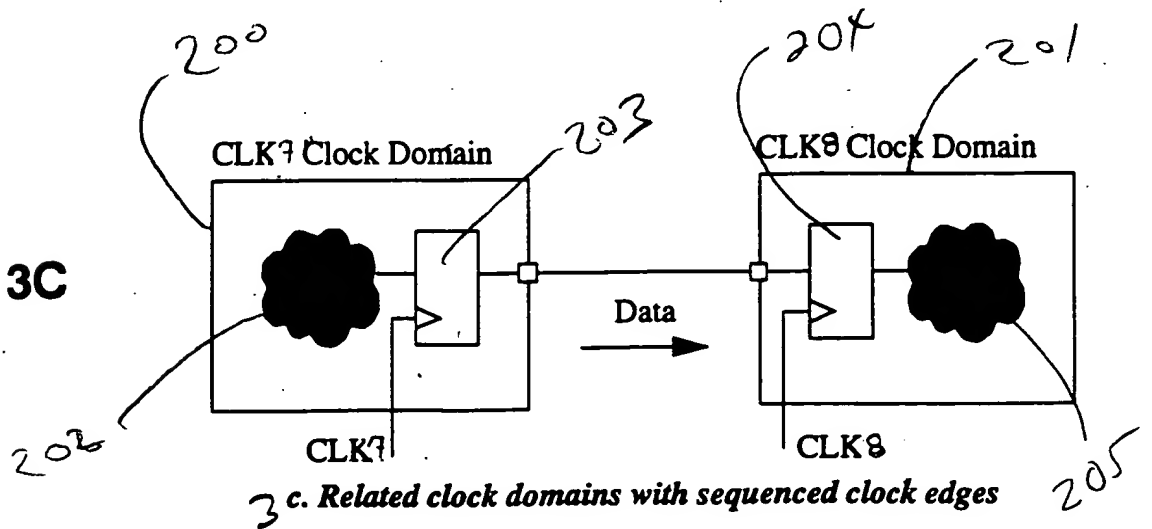


FIGURE 5

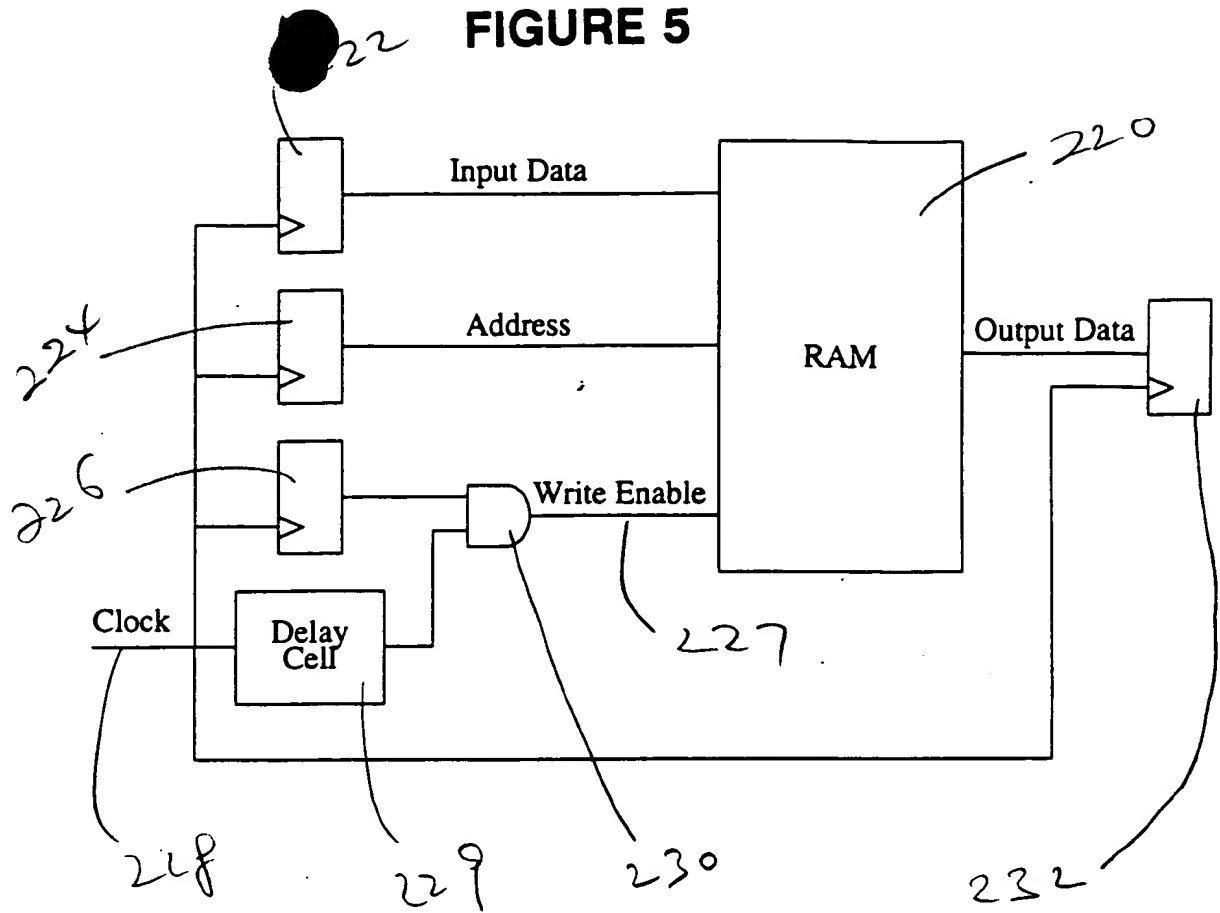


FIGURE 6

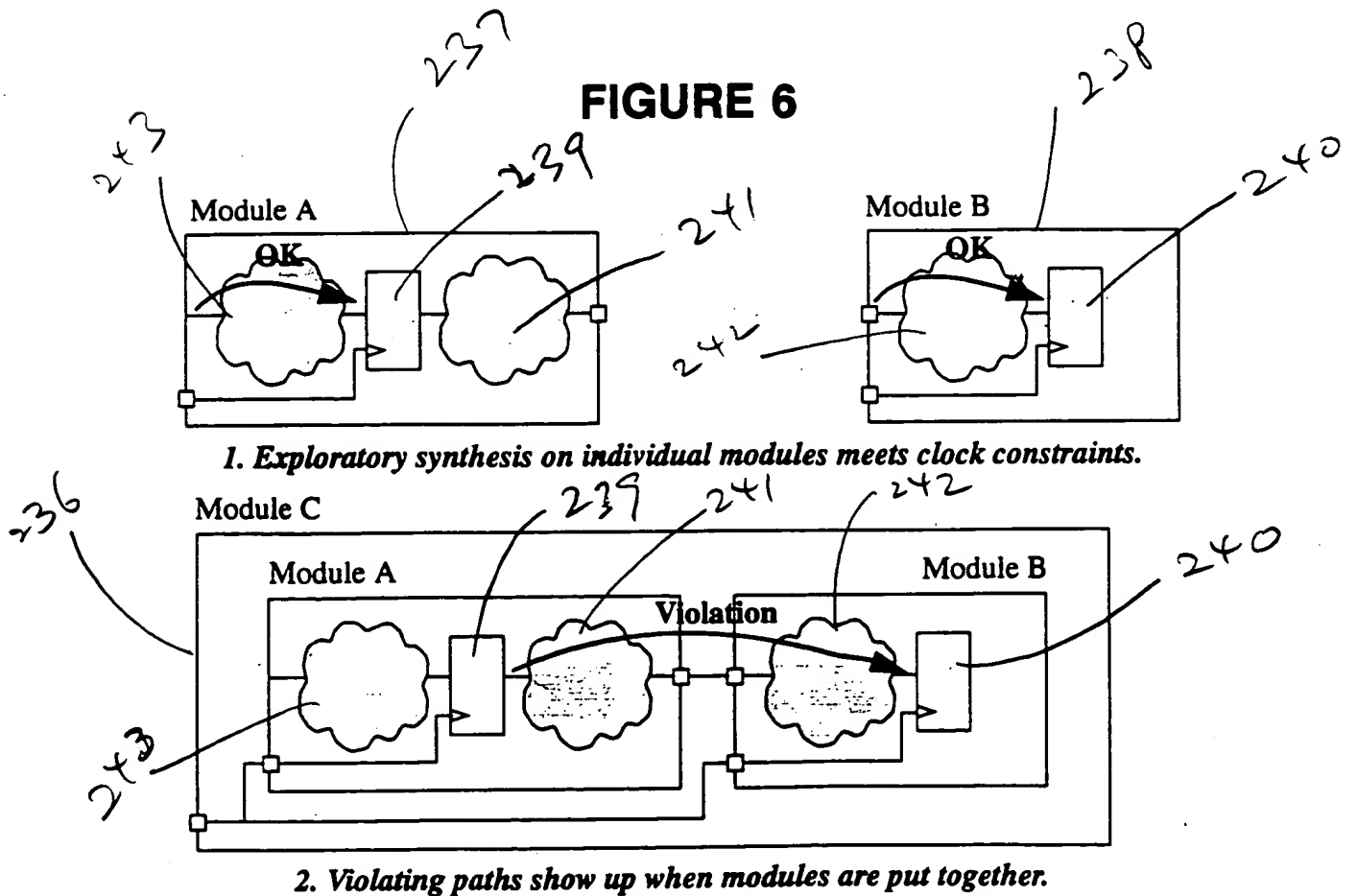


FIGURE 7

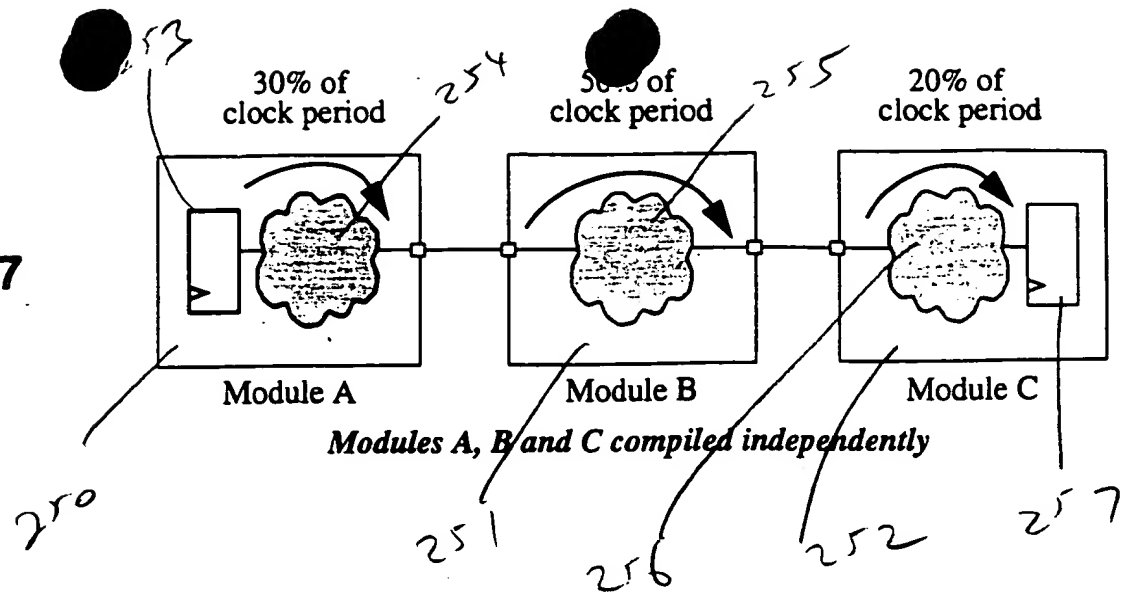


FIGURE 8

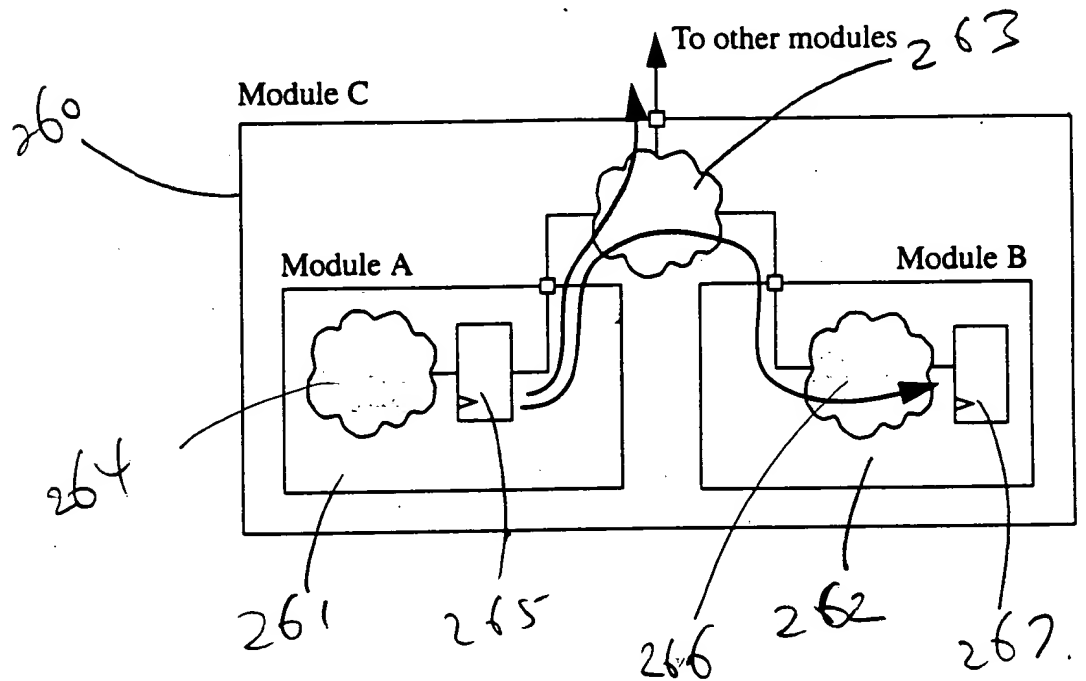


FIGURE 9

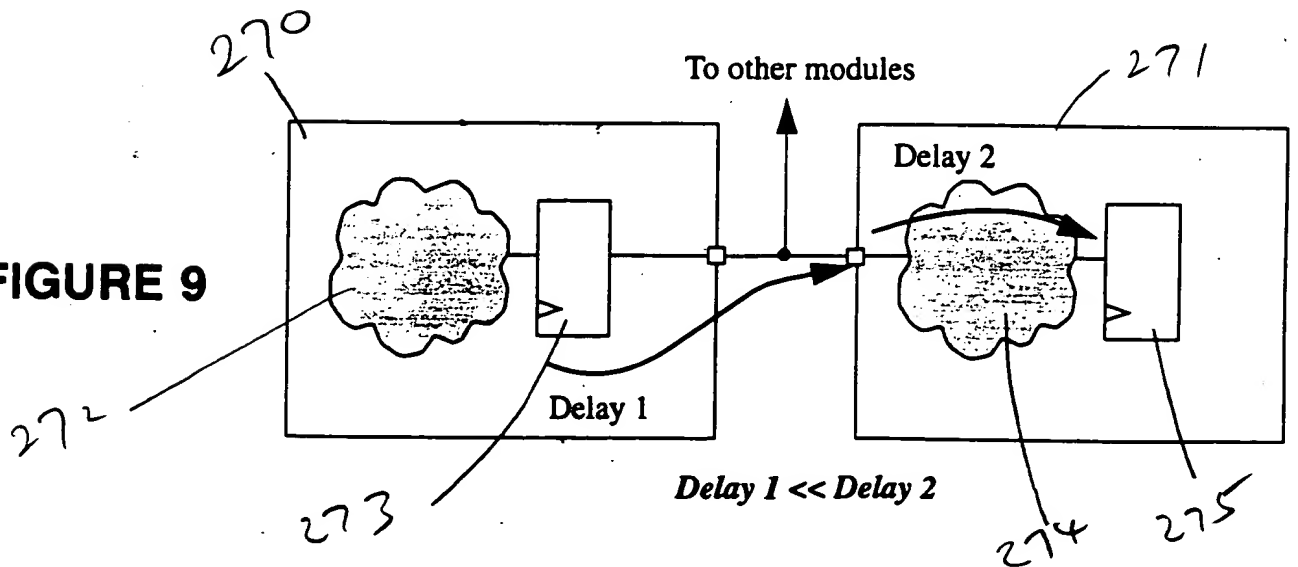


FIGURE 10A

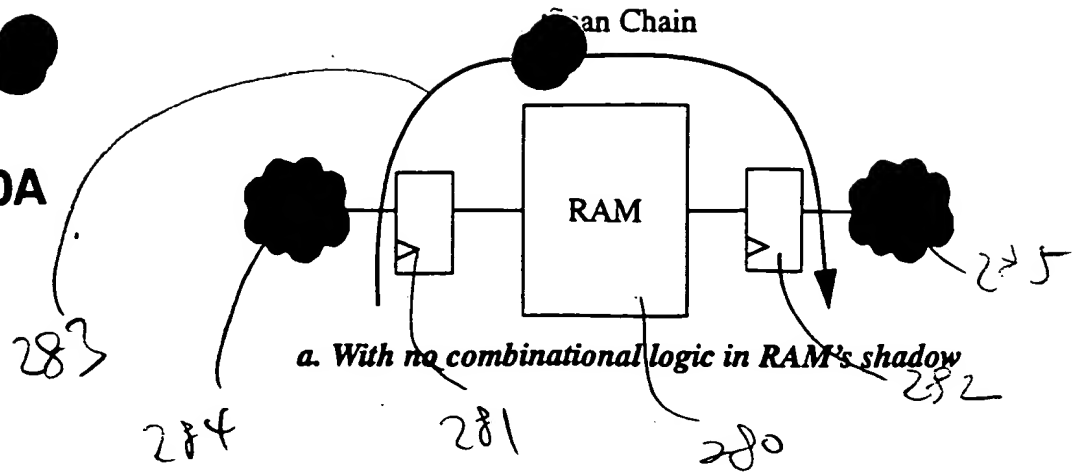


FIGURE 10B

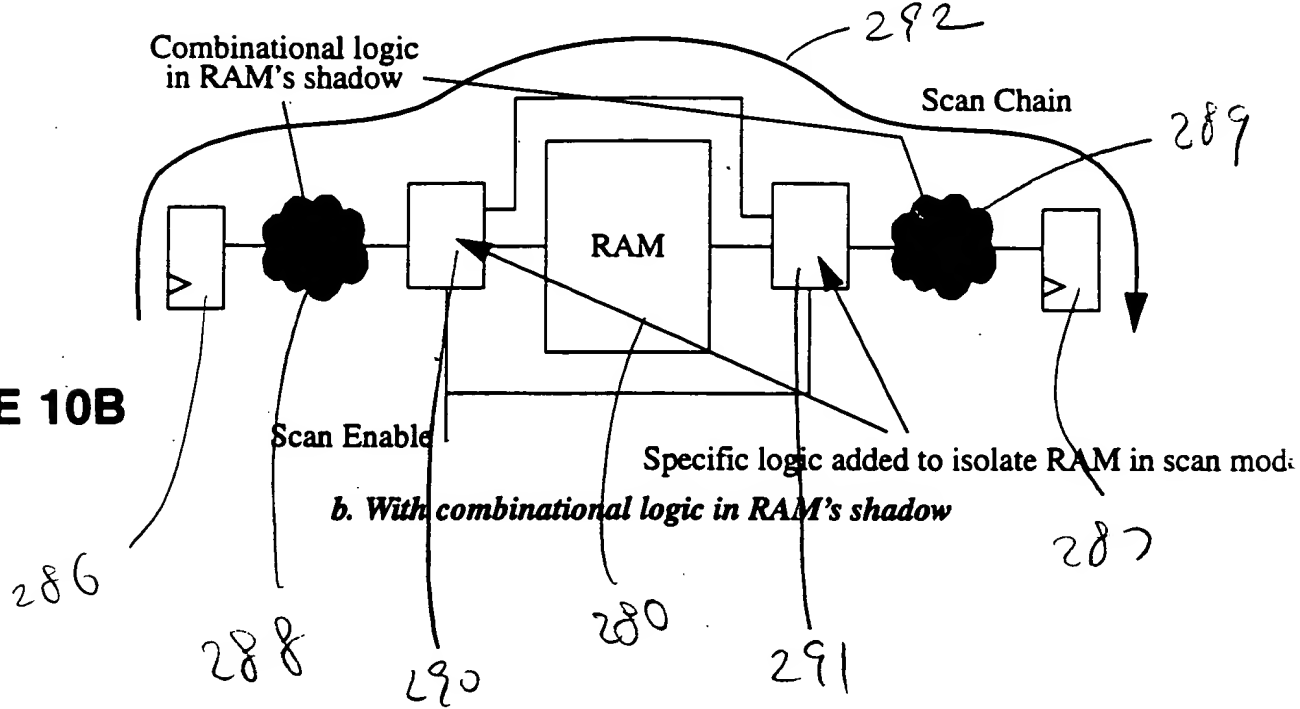


FIGURE 11

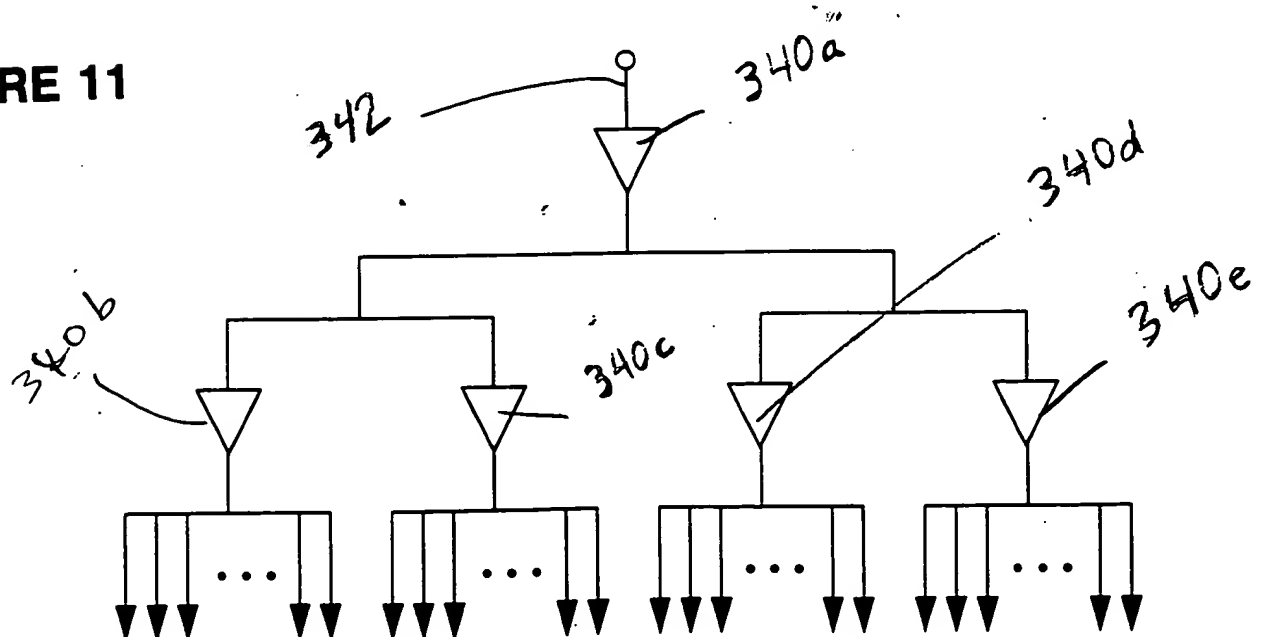
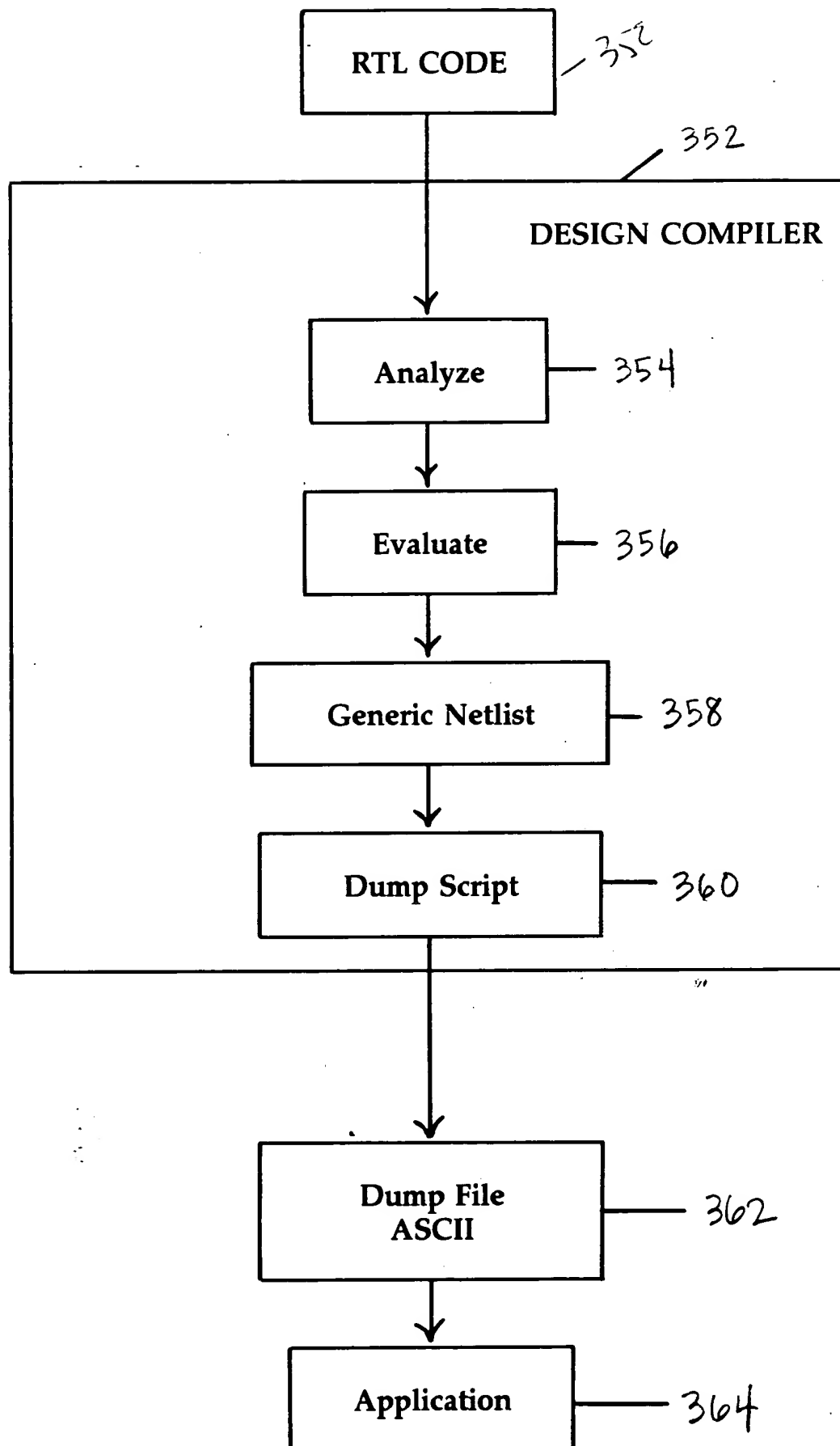


FIGURE 12



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FIGURE 13

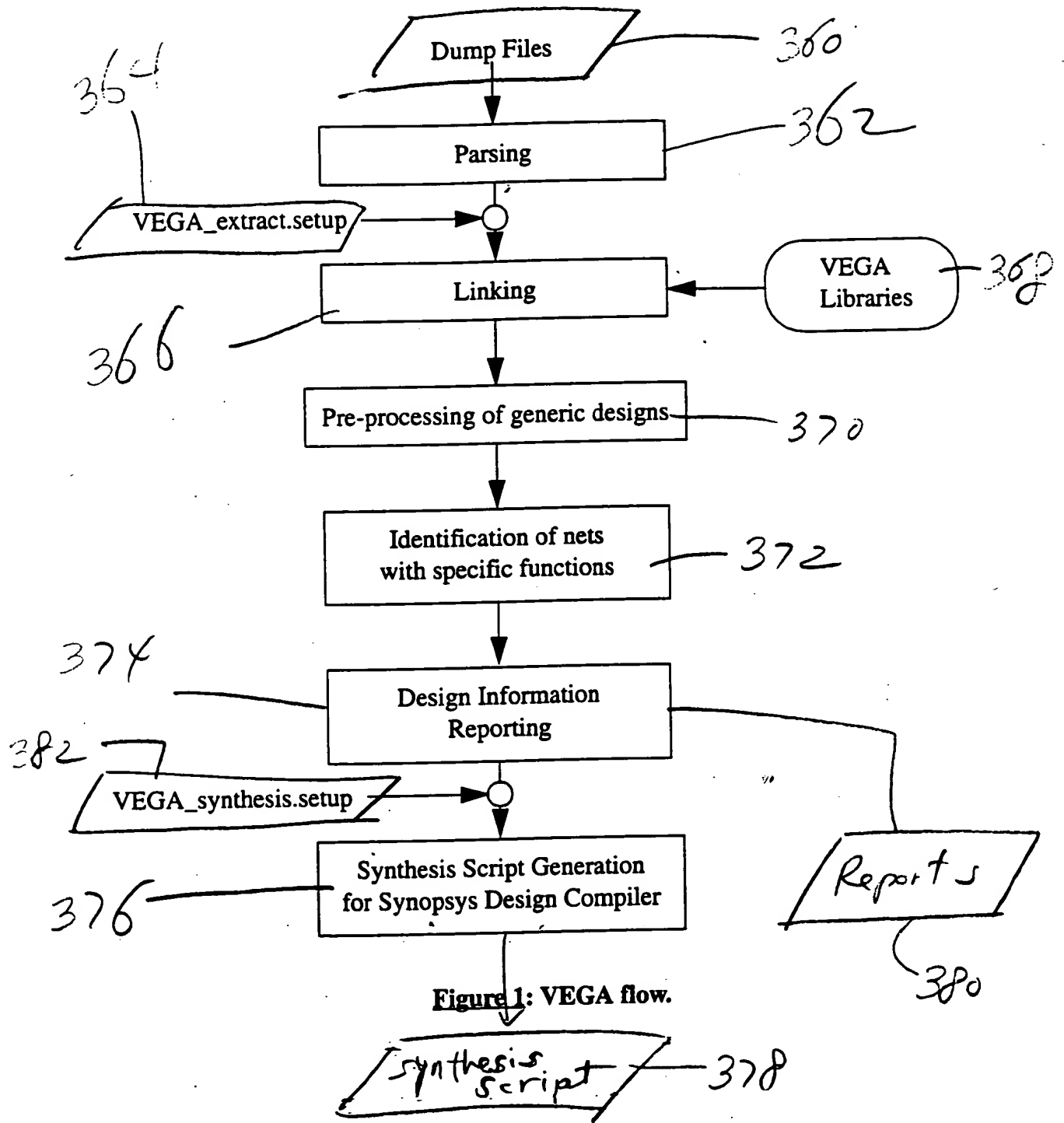
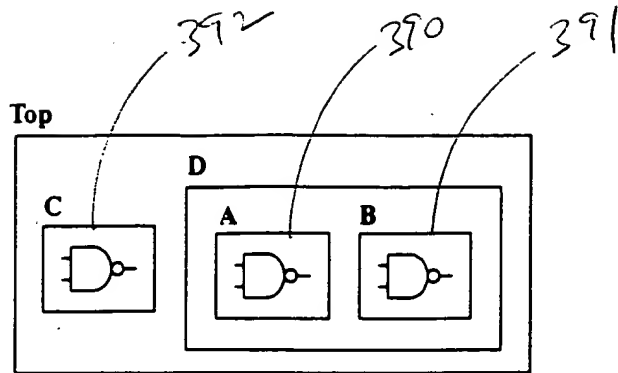
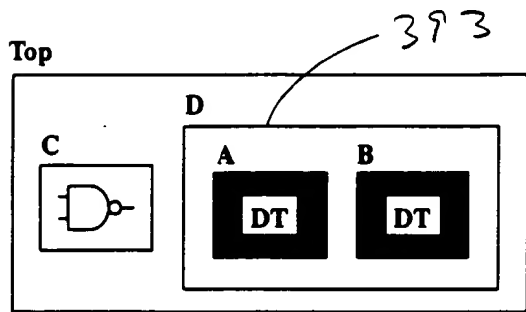


Figure 1: VEGA flow.

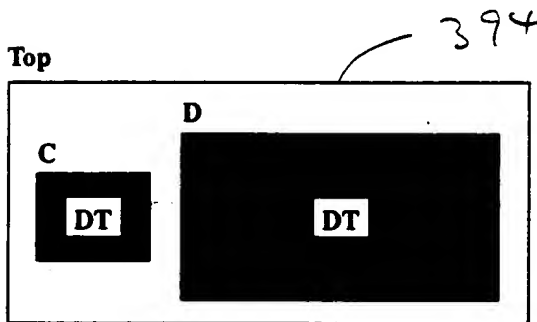
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Step #1: Leaf modules A, B, and C are synthesized.



Step #2: Module D is synthesized with modules A and B made non-modifiable (dont-touch attributes).



Step #3: Module TOP is synthesized with modules C and D made non-modifiable.

FIGURE 14 : Bottom-up synthesis.

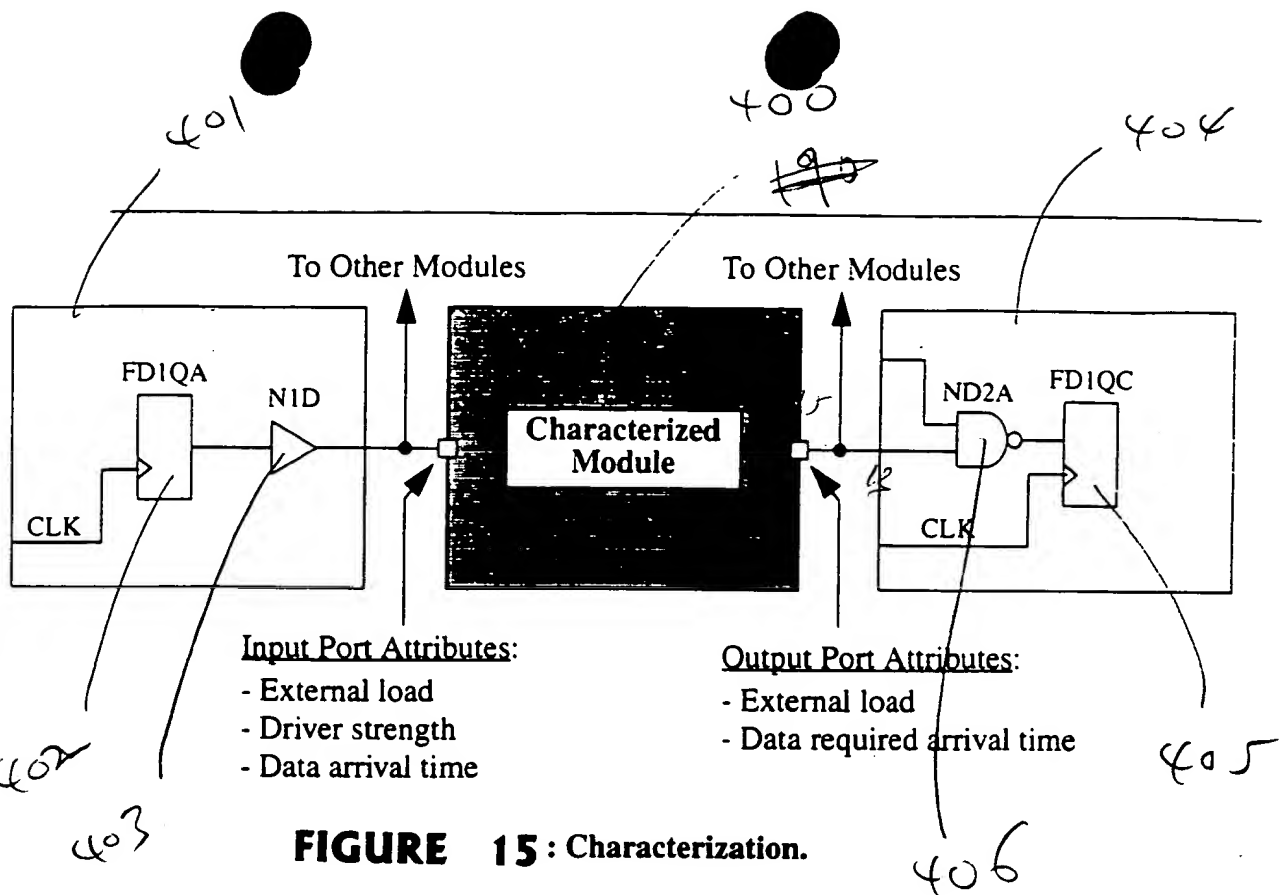


FIGURE 15 : Characterization.

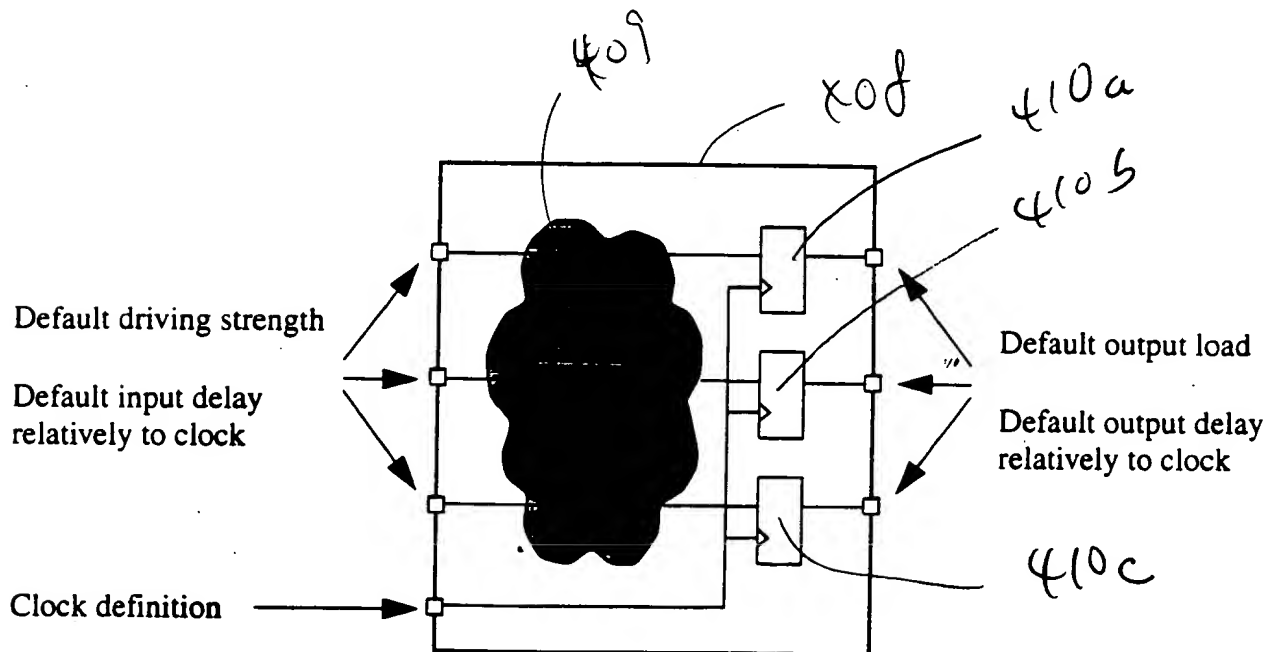
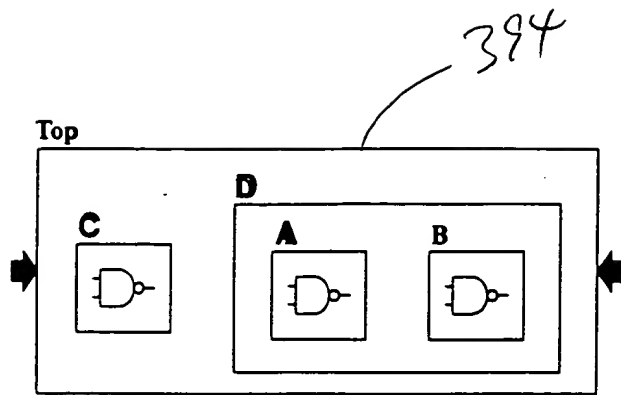
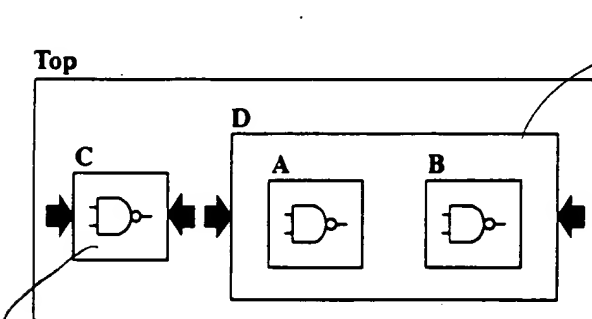


FIGURE 17 : Default constraints used for initial mapping.

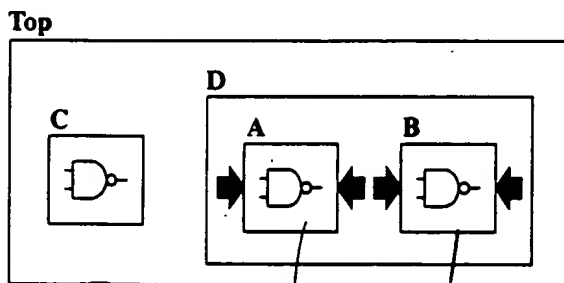


Step #1: Constraints are set on top-level module (operating conditions, clock definitions, ect).



Step #2: Constraints are derived on modules C and D.

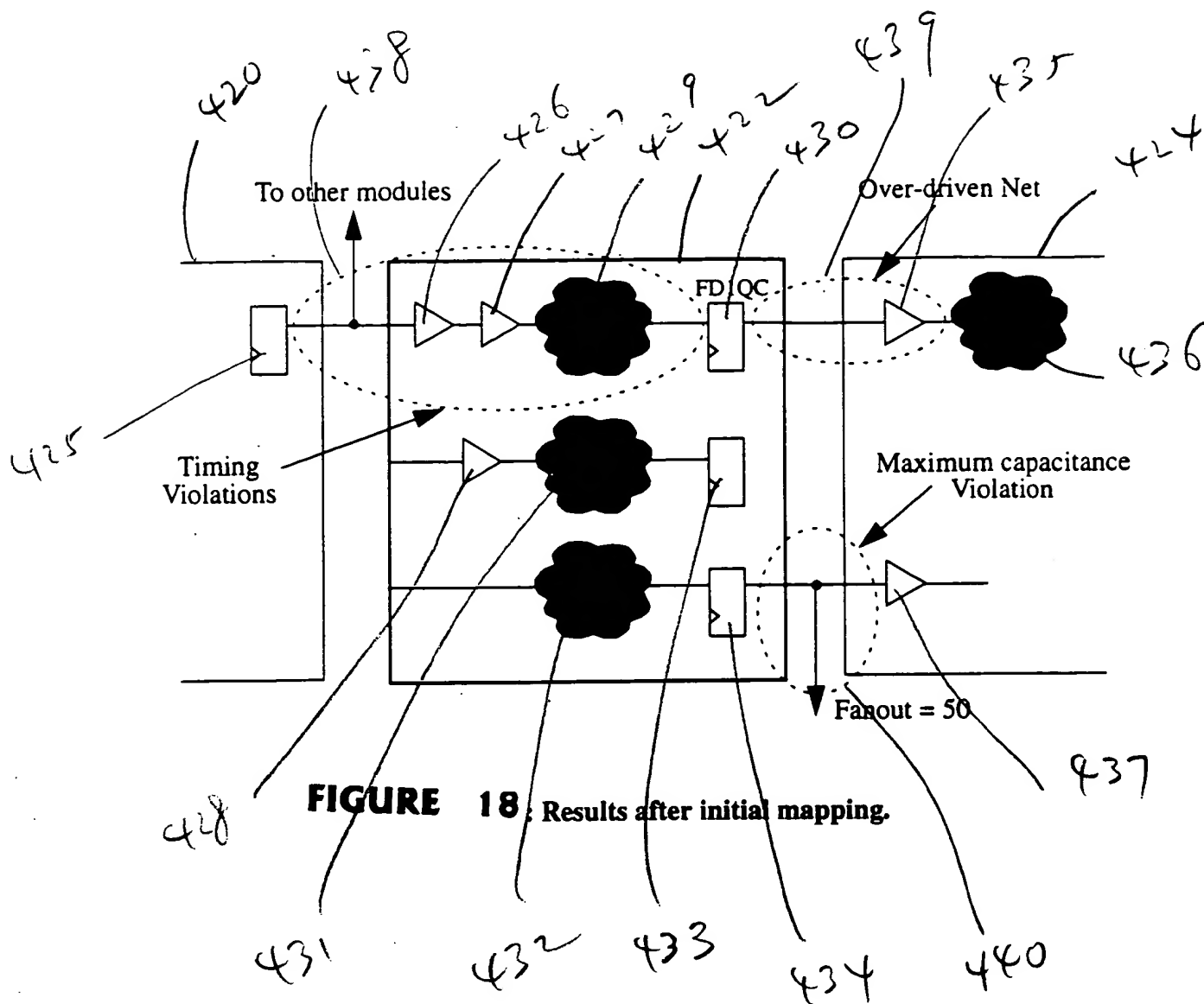
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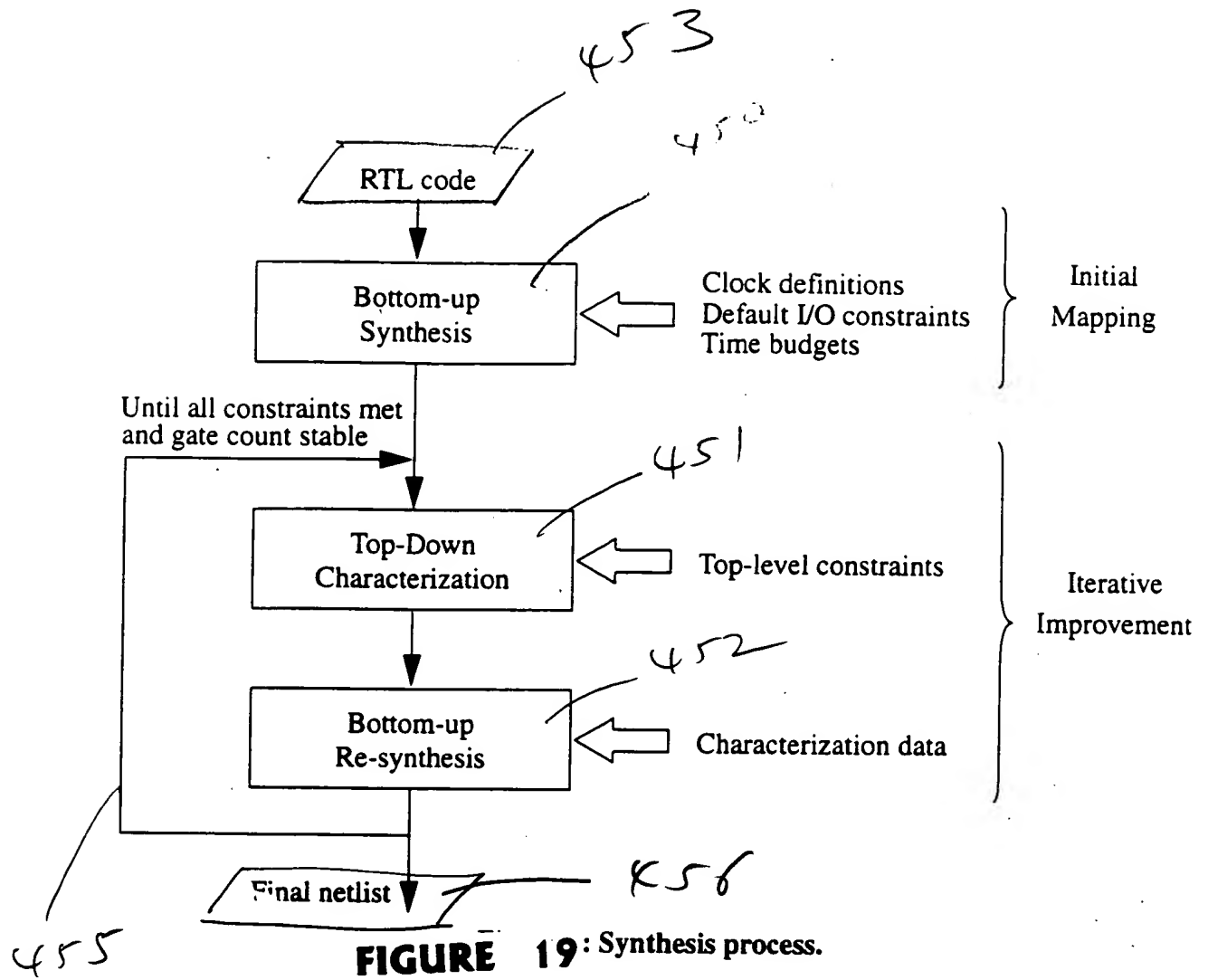


Step #3: Constraints are derived on leaf modules A and B.

FIGURE 16: Top-down characterization.

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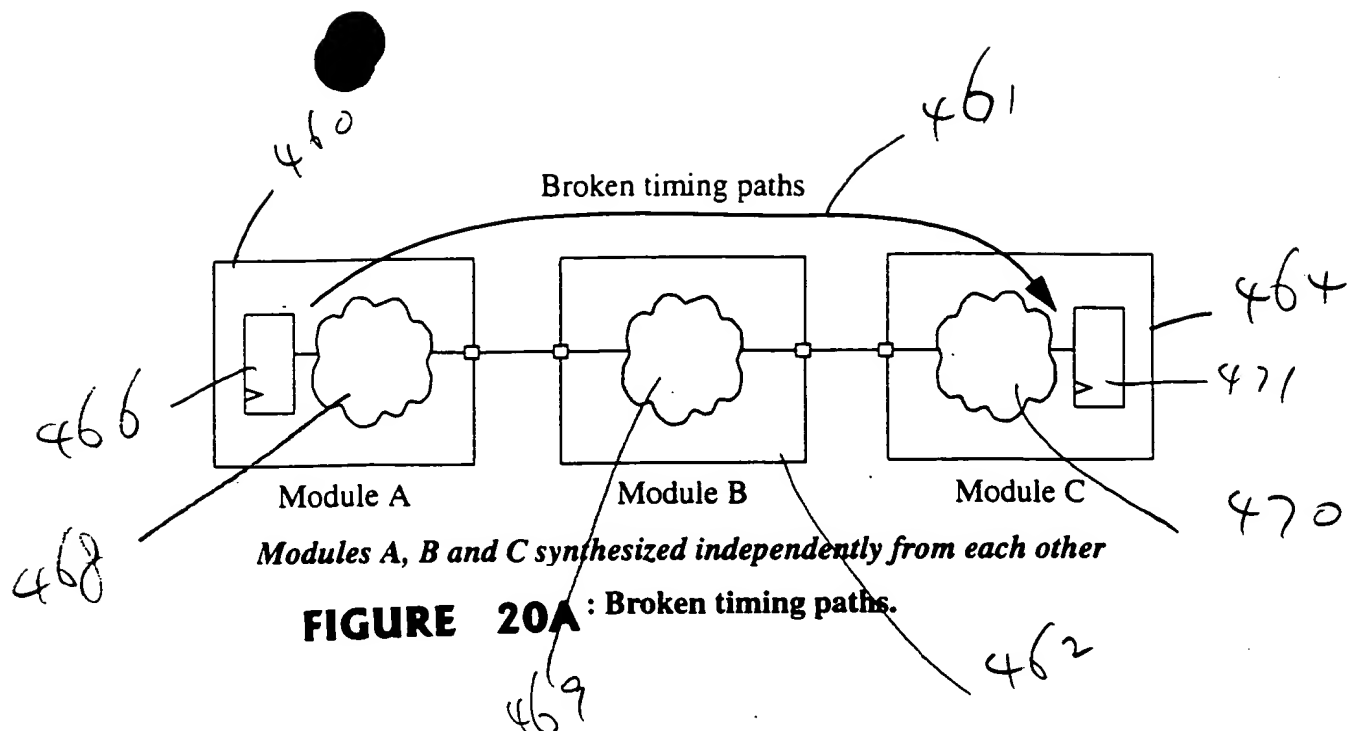
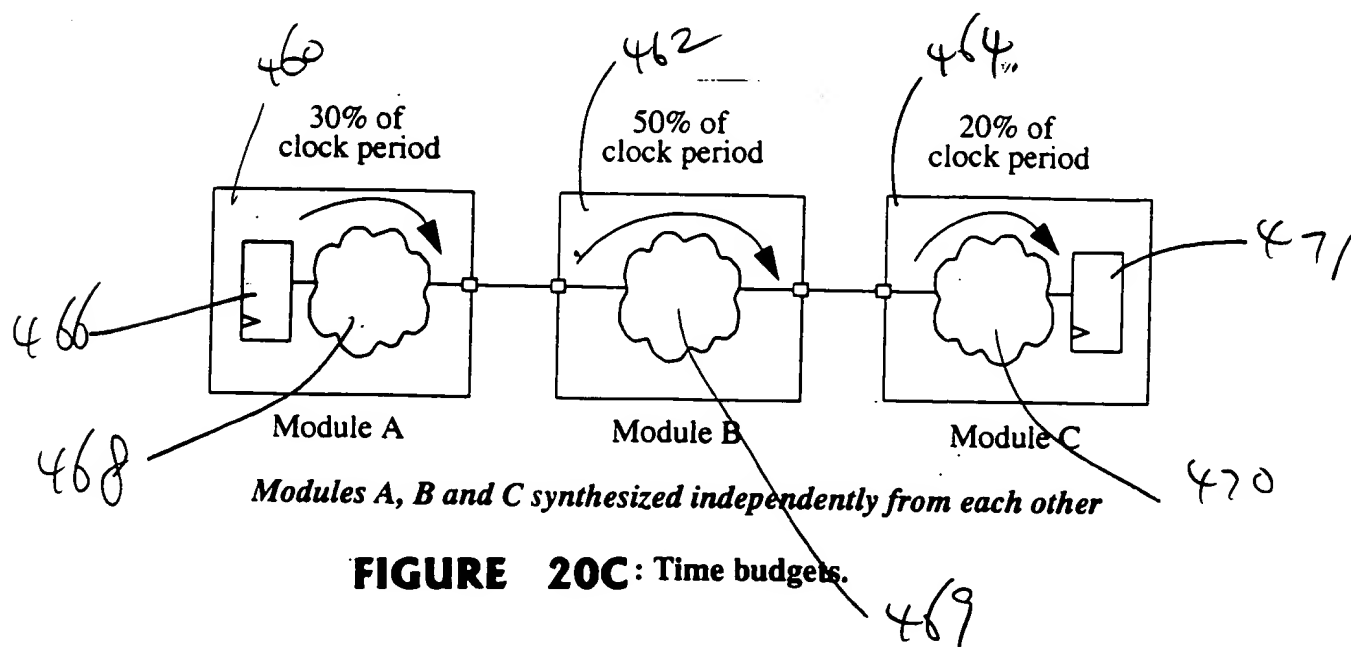


FIGURE 20B: In the absence of broken timing paths.



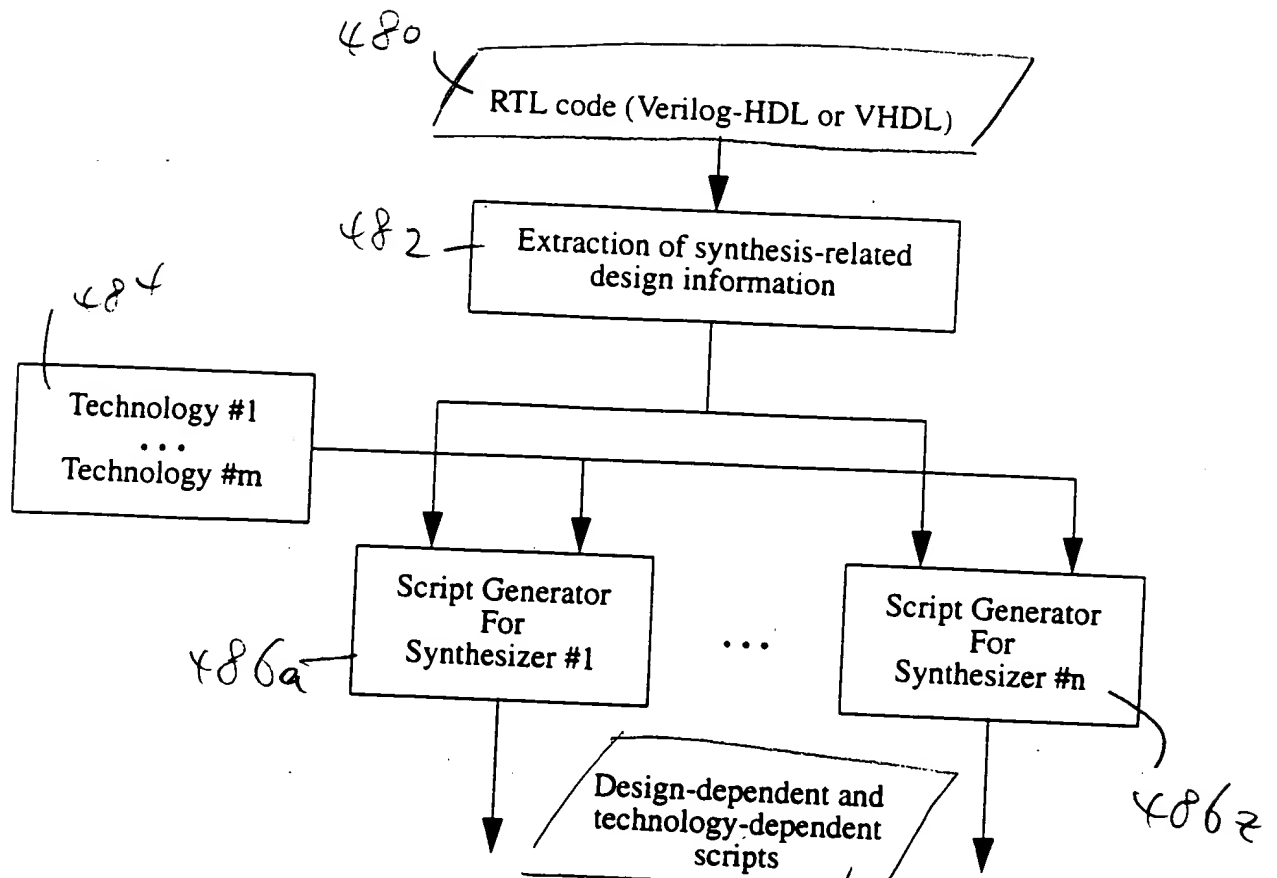


FIGURE 21 : Automatic script generation.

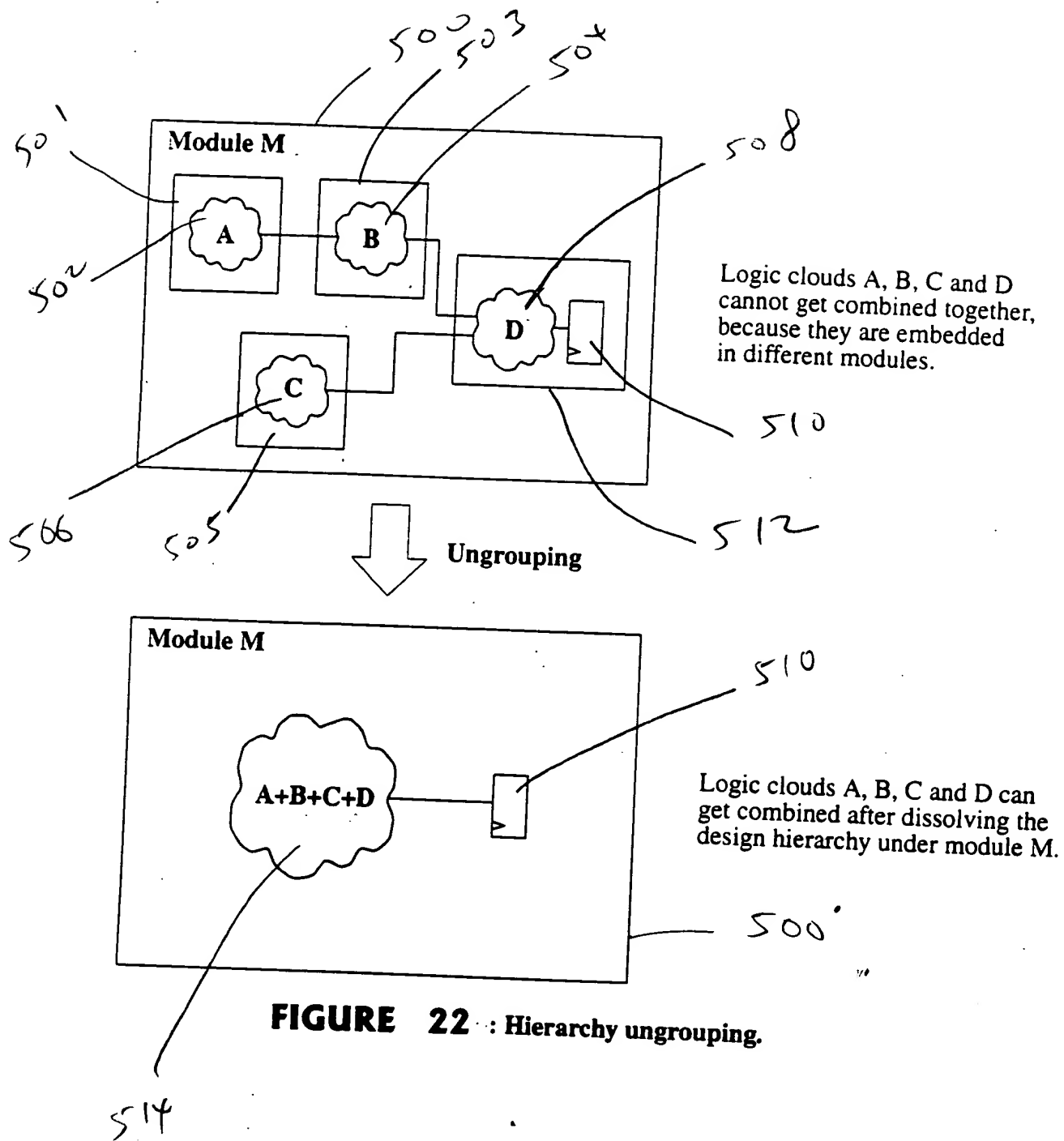
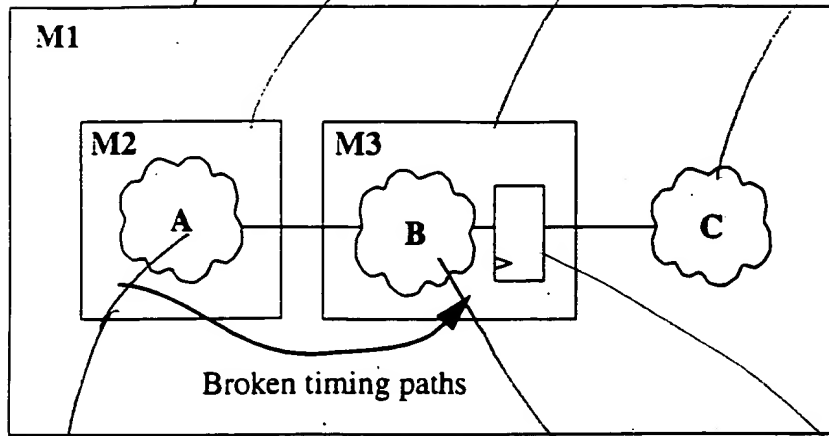
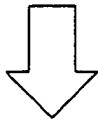


FIGURE 22 : Hierarchy ungrouping.

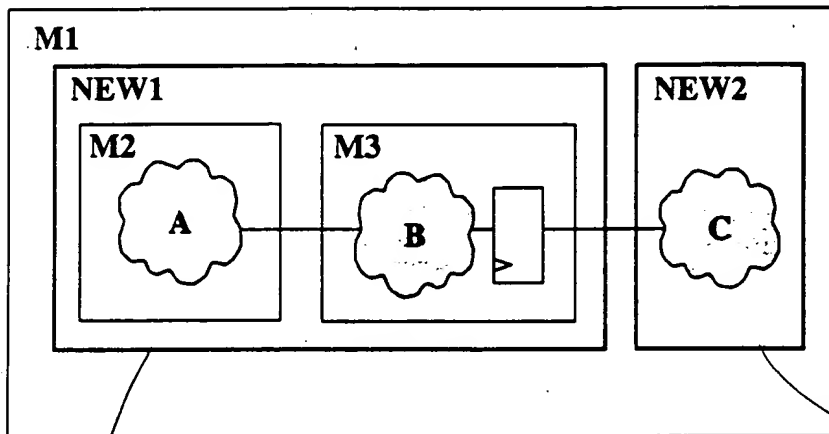


Broken timing paths run through modules M2 and M3.

Module M1 mixes hierarchy (modules M2 and M3) with logic (cloud C).



Grouping



M2-M3 timing paths are now fully contained in new module NEW1.

If modules M2 and M3 are small enough, the hierarchy can be dissolved below NEW1.

New module NEW2 encapsulates cloud of logic C.

FIGURE 23 : Hierarchy grouping.

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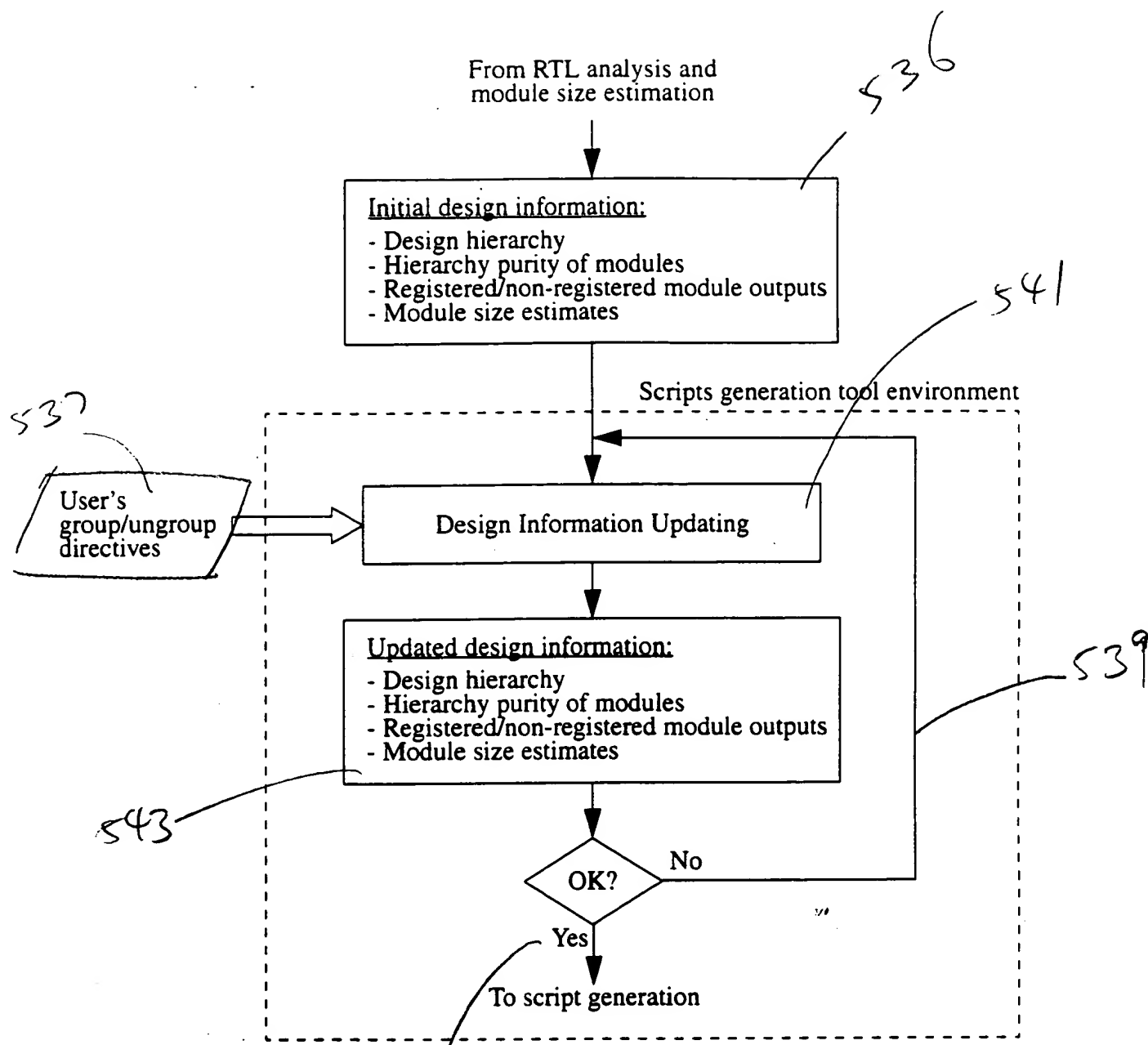


FIGURE 24 : Support for design hierarchy re-arrangement.

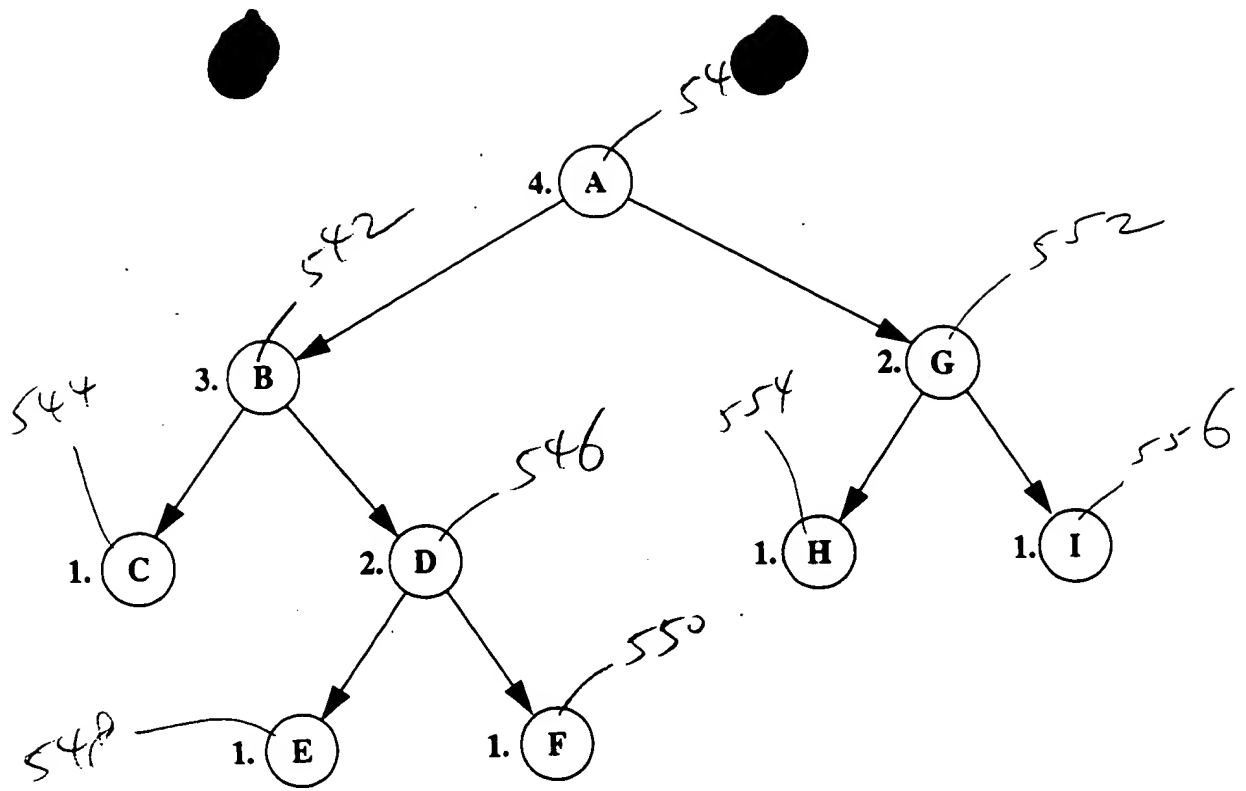


FIGURE 25 : Module processing order for parallel bottom-up synthesis.

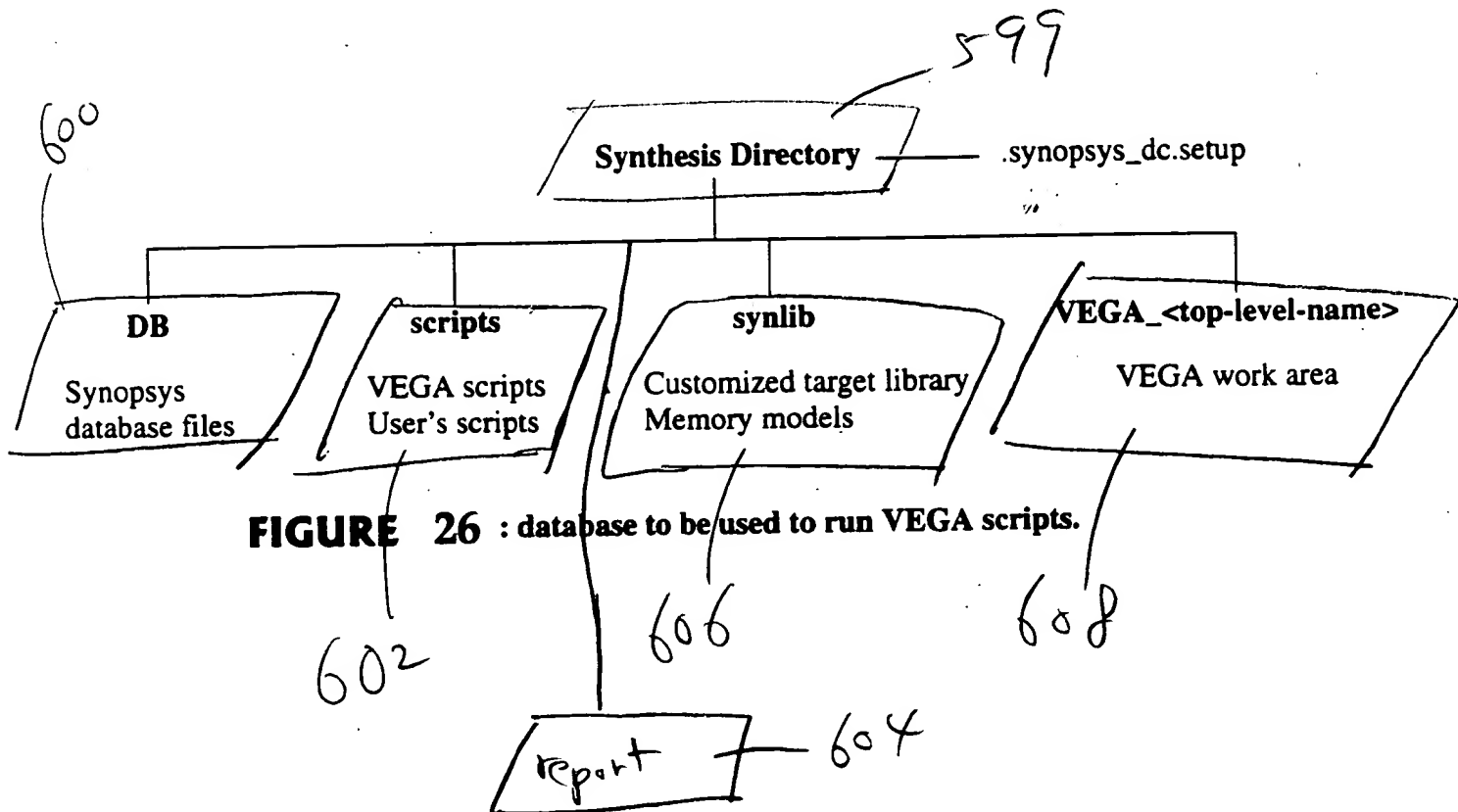
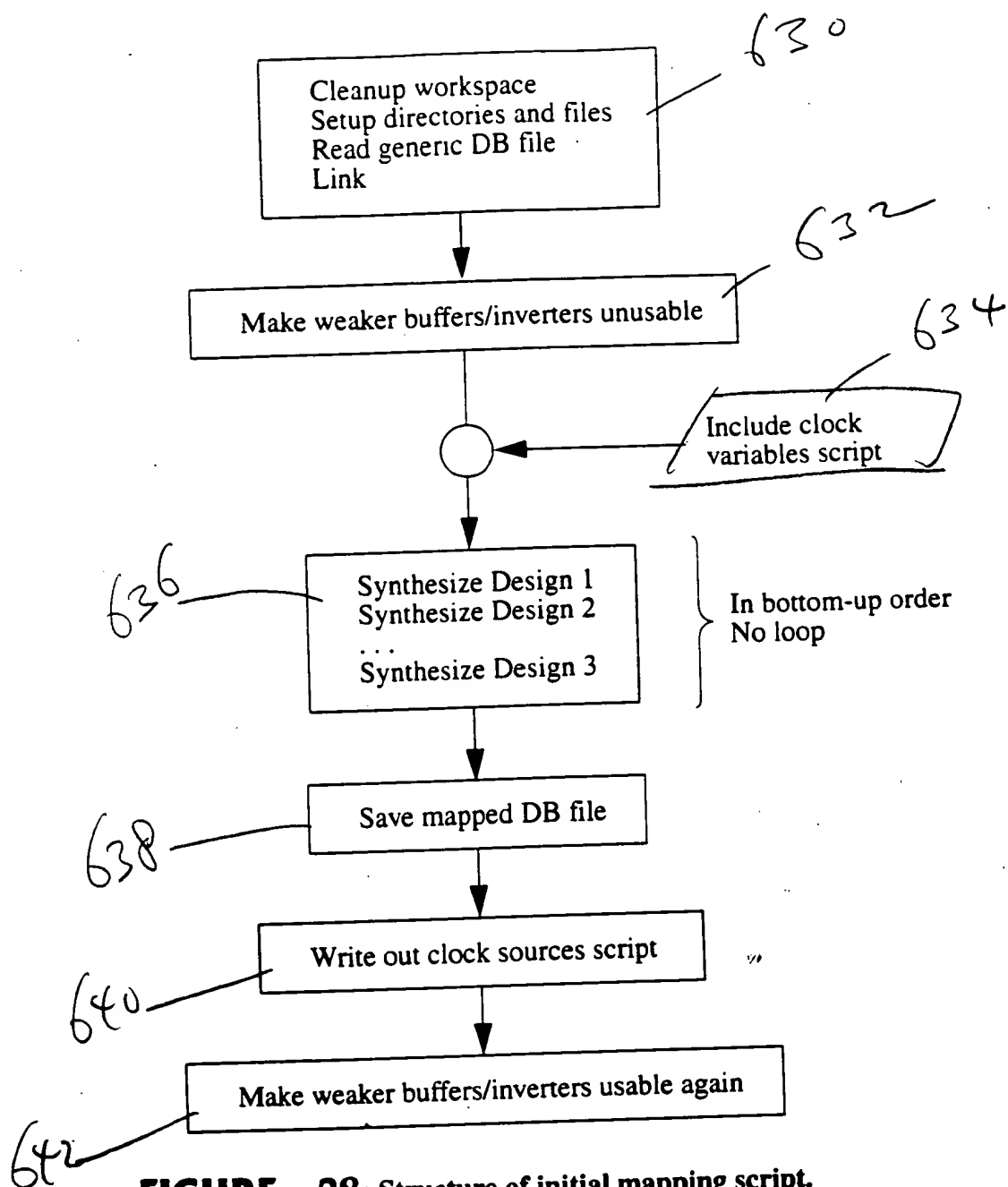


FIGURE 26 : database to be used to run VEGA scripts.



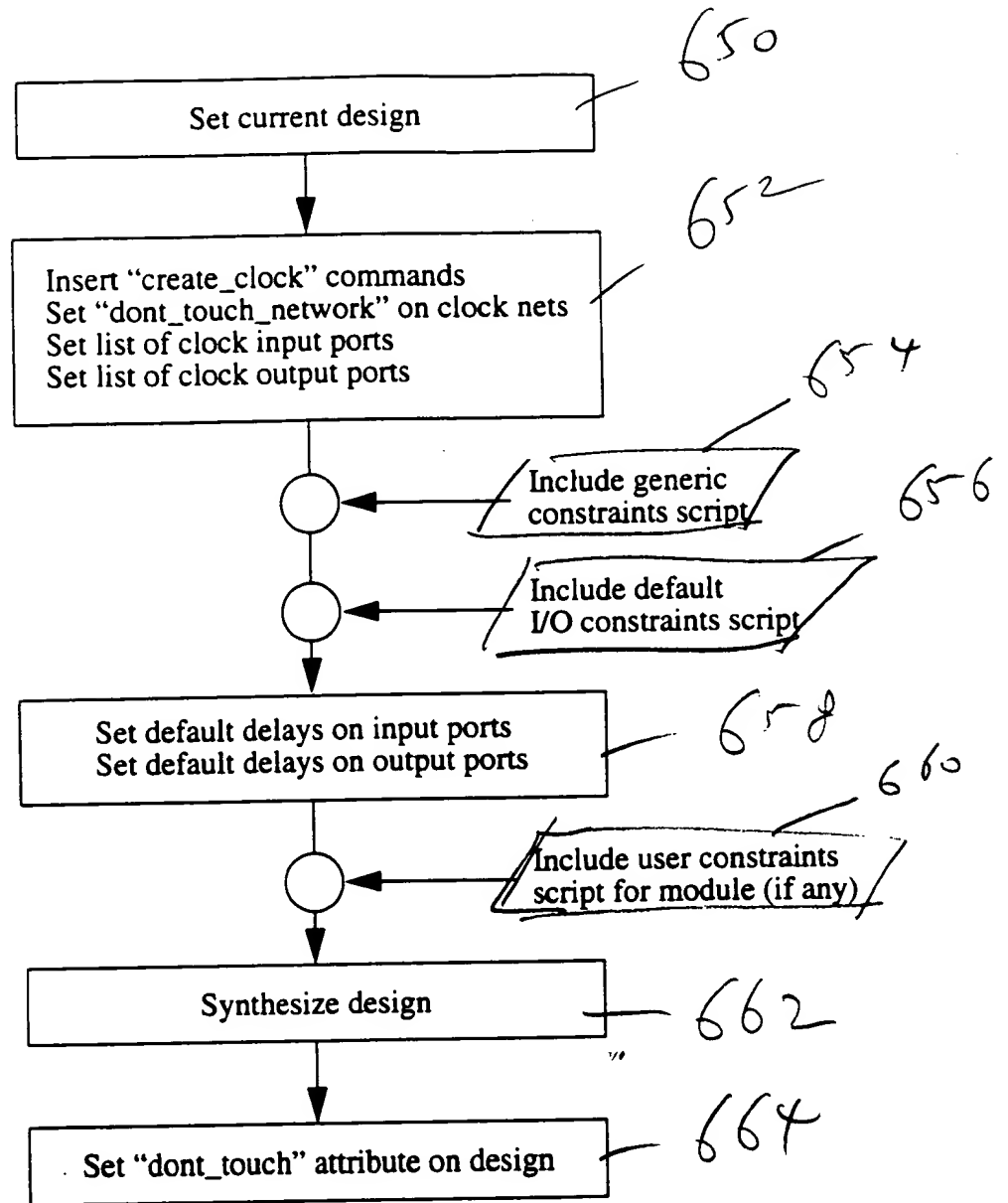


FIGURE 29 : Operations performed on each module by initial mapping.

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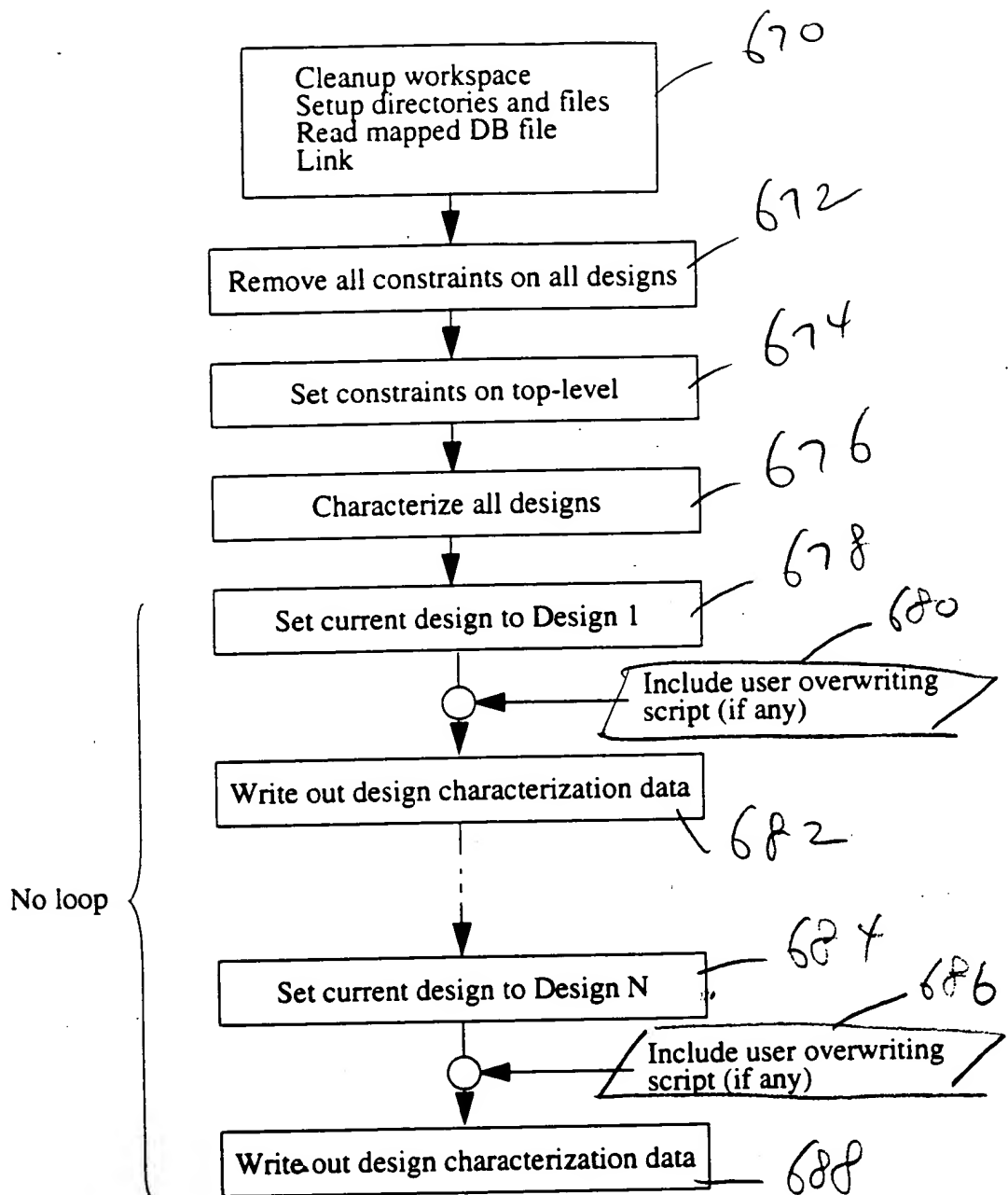


FIGURE 30 : Structure of characterization script.

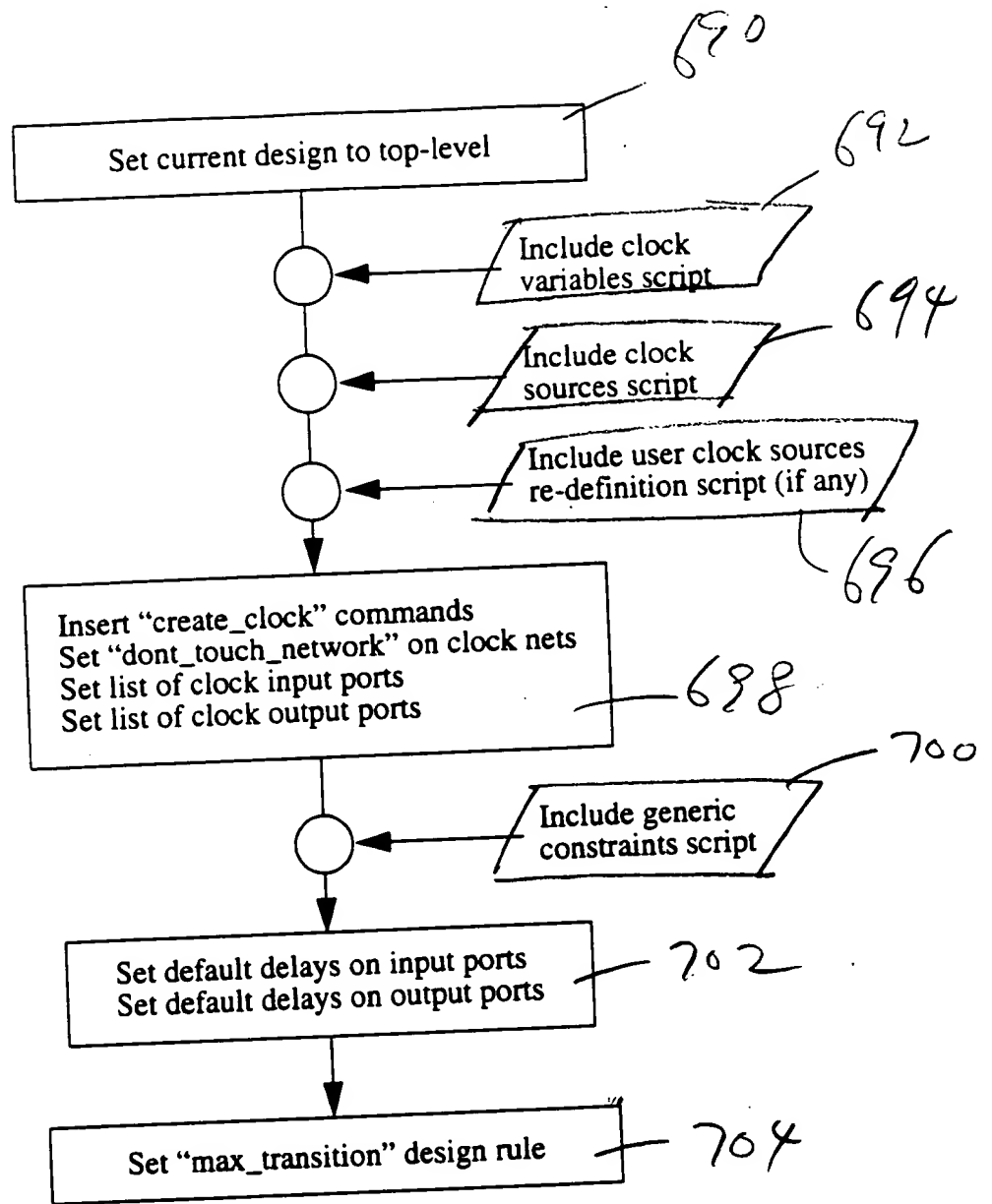


FIGURE 31 : Structure of constraints setting on top-level.

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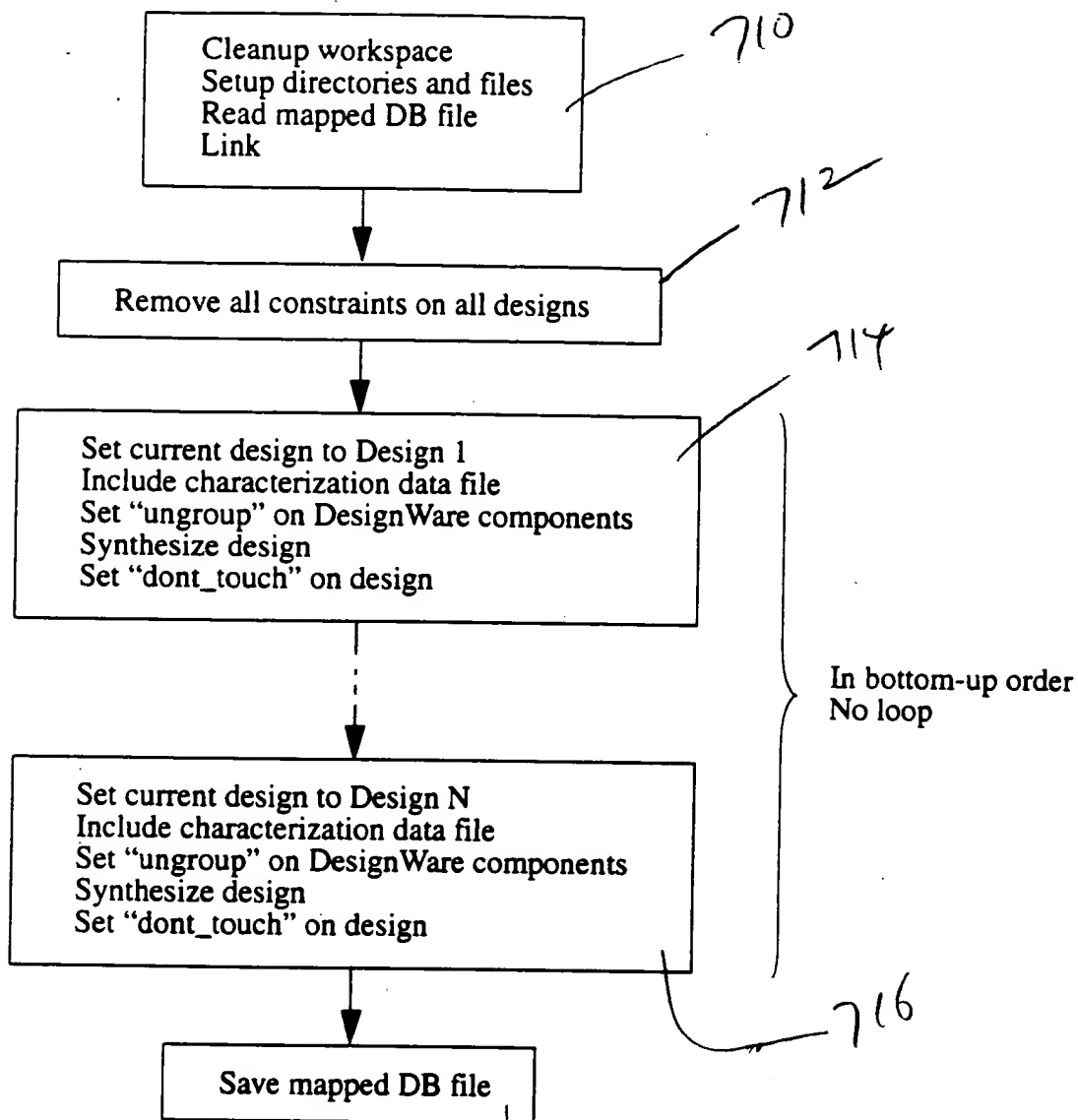


FIGURE 32 : Structure of re-synthesis script.

```

always (posedge INT_CLK)
begin
  if (~SEL)
    Z = D0;
  else
    Z = D1;
end

always @(CLK or GCLK)
  assign INT_CLK = CLK & GCLK;

```

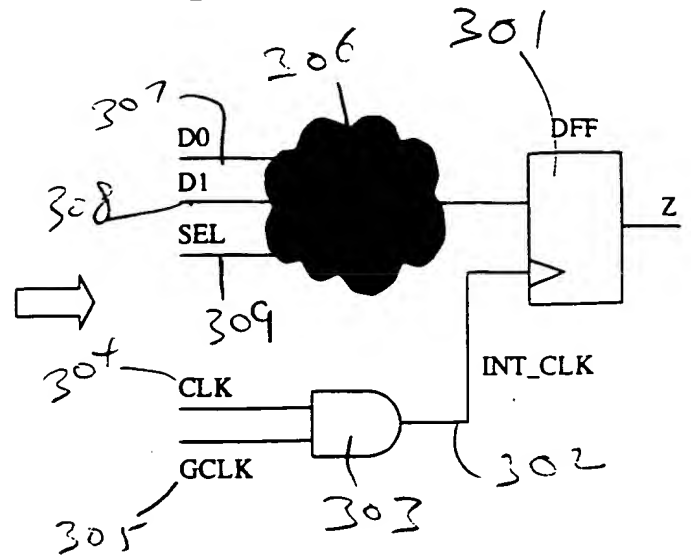


FIGURE 33 : Example of RTL code and equivalent Hardware view for RTL analysis.

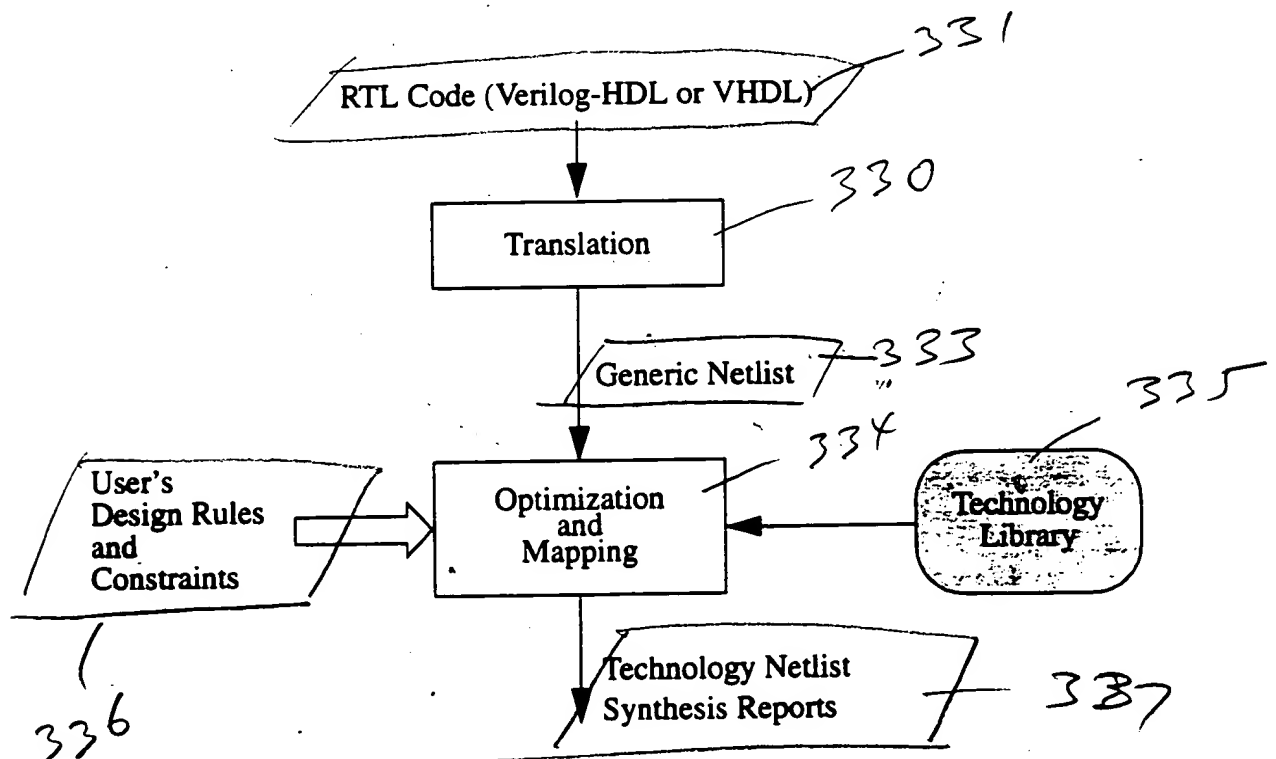


FIGURE 36 : Logic synthesis process

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```
process(RESET_N, CLK)
begin
    if (RESET_N = '0') THEN
        Q1 <= '0';
    elsif CLK'event AND (CLK = '1') THEN
        Q1 <= D1;
        Q2 <= D2;
    endif;
end process;
```

a. VHDL code for a 2-bit register with partial asynchronous reset

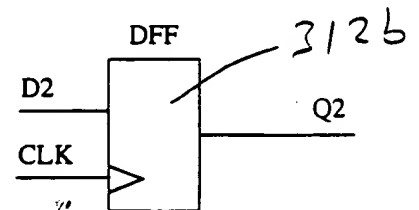
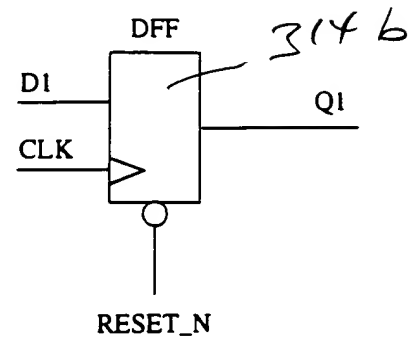
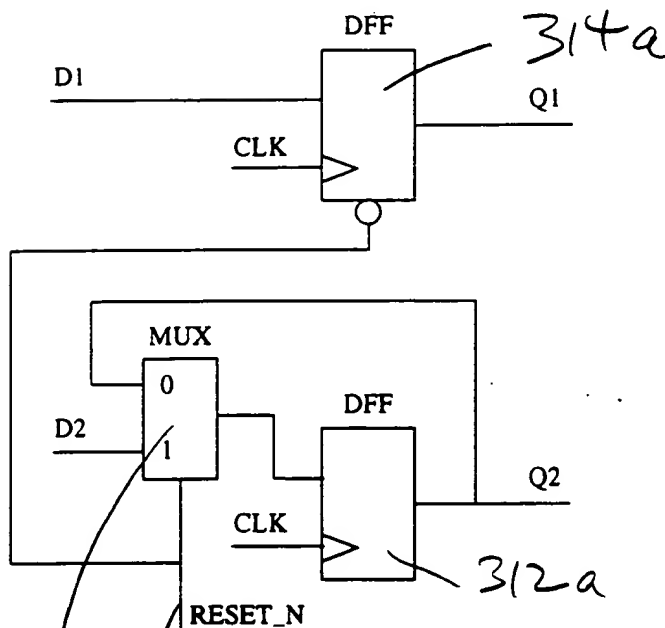


FIGURE 34B

b. Implementation created by Synopsys Design Compiler.

FIGURE 34 C

c. Implementation created by AMBIT BuildGates

: Implementation of partial asynchronous reset.

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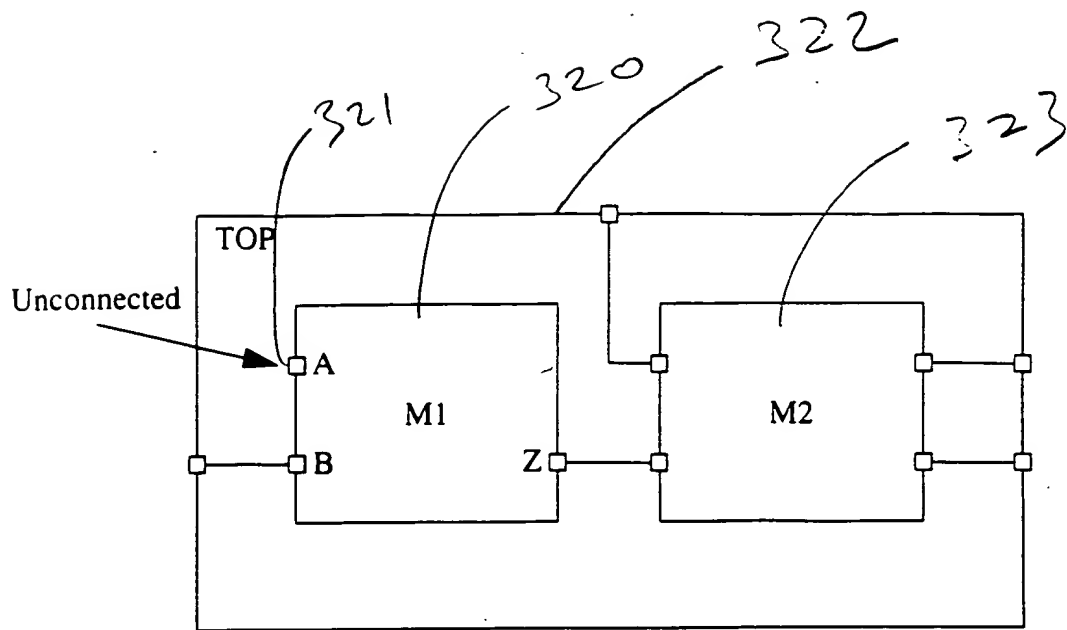


FIGURE 35A . RTL code

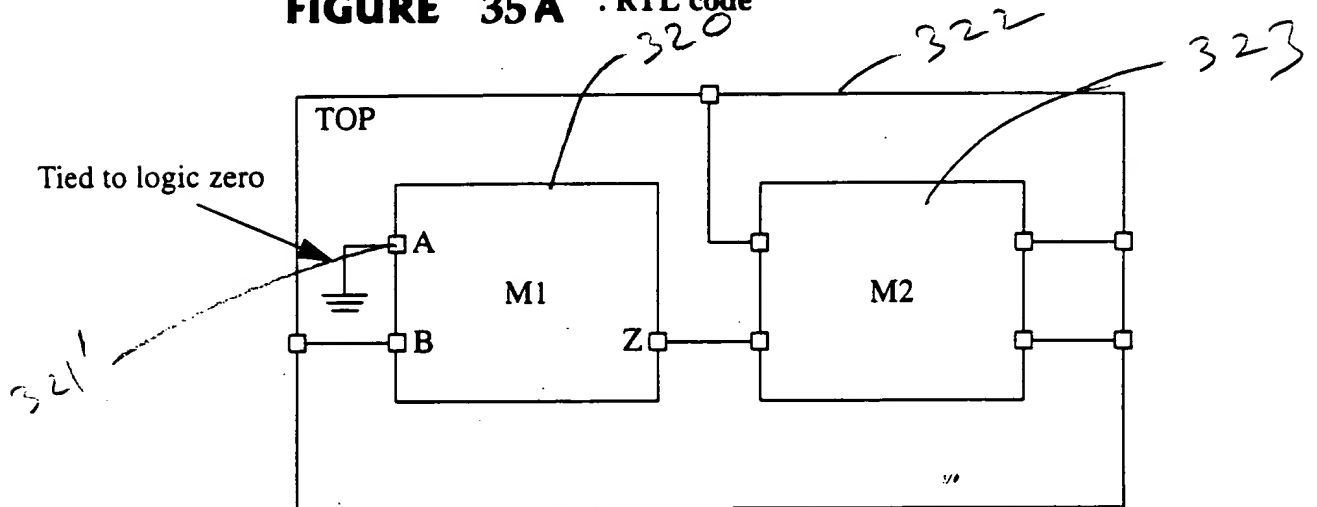


FIGURE 35 B Synopsys Design Compiler view of the RTL code

; Handling of unconnected module input pins by Synopsys Design Compiler.

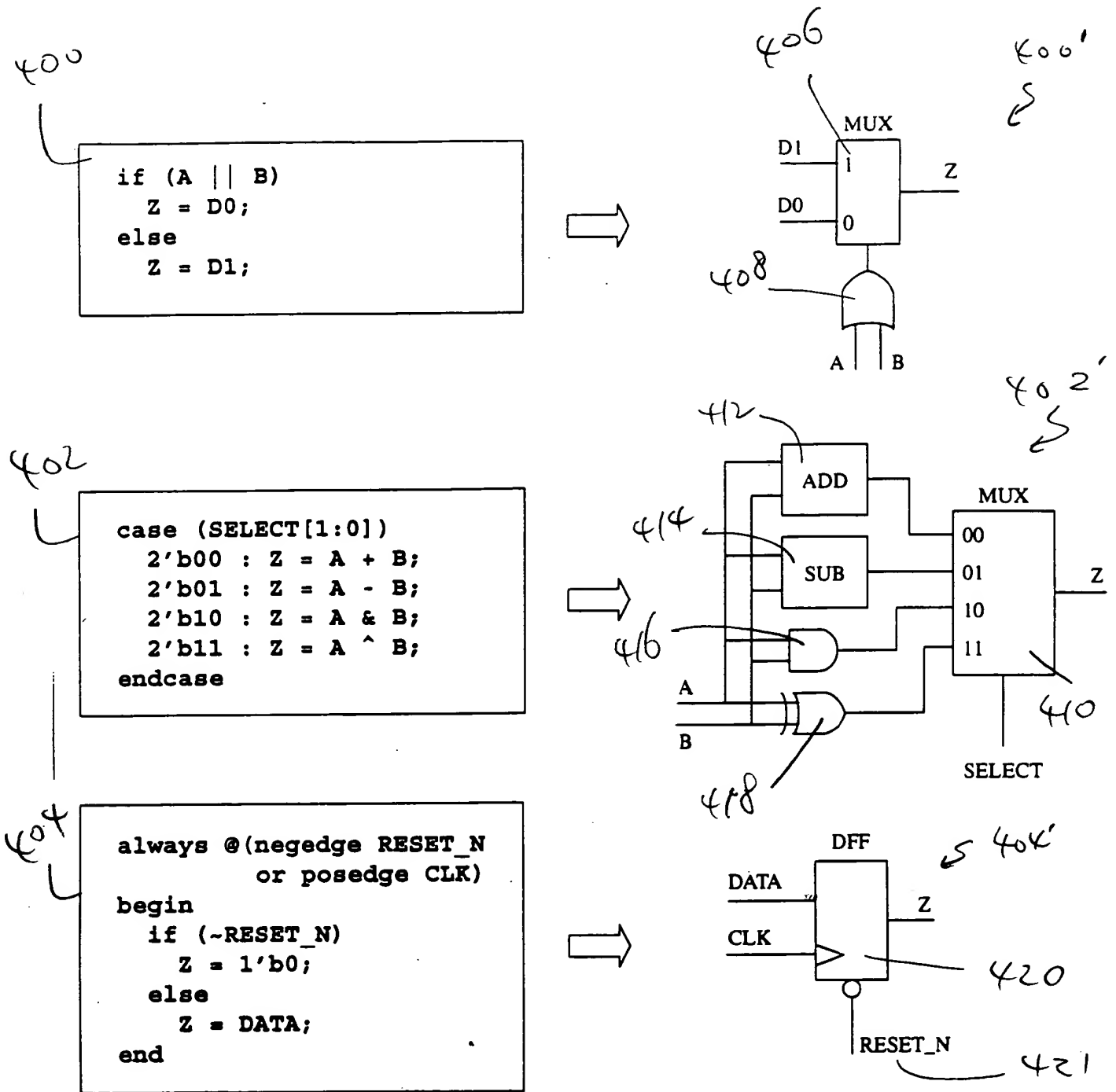


FIGURE 38 : Examples of transforms used for RTL code translation.

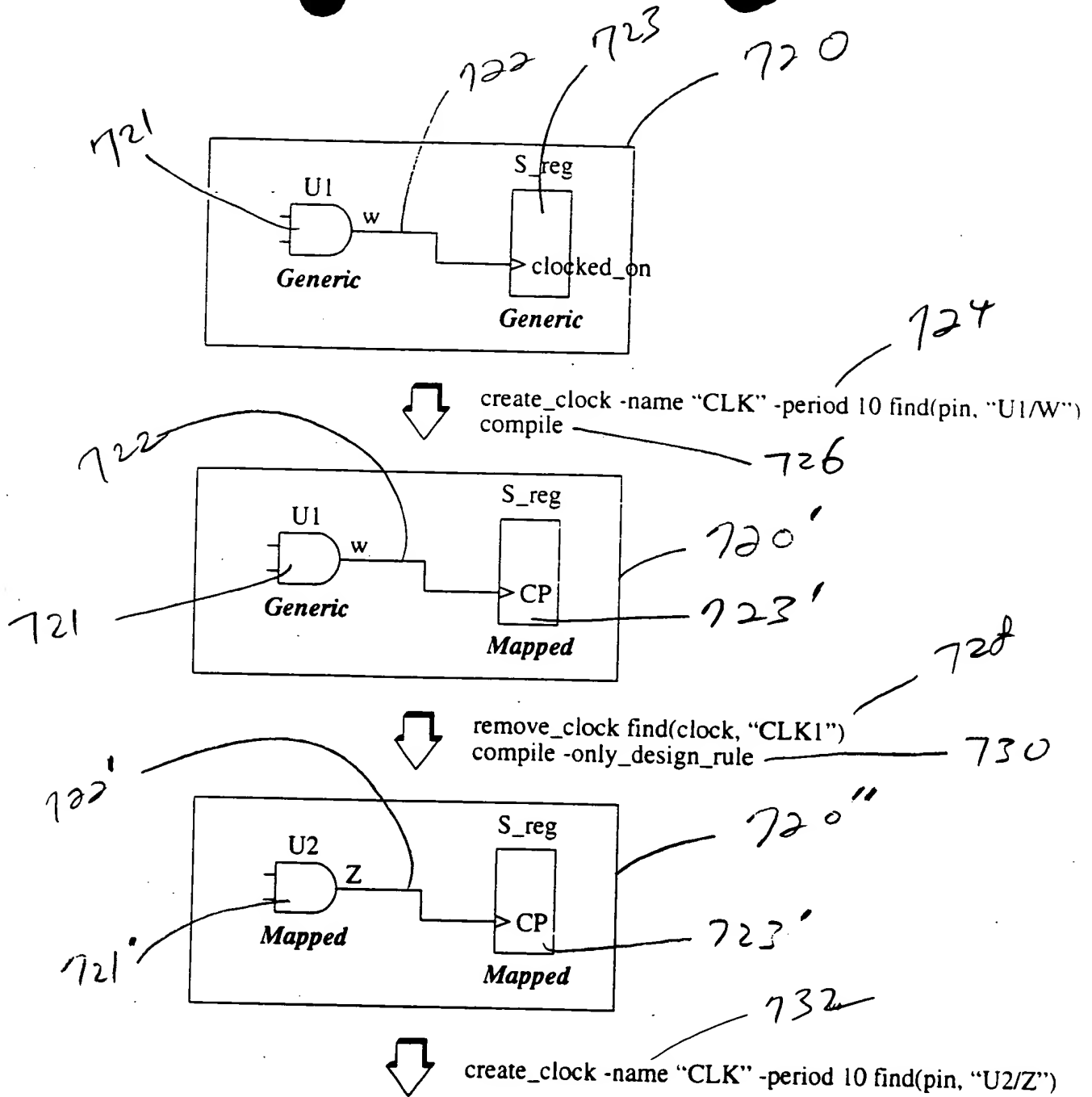


FIGURE 40 : Process used to map cells that create internal clocks.

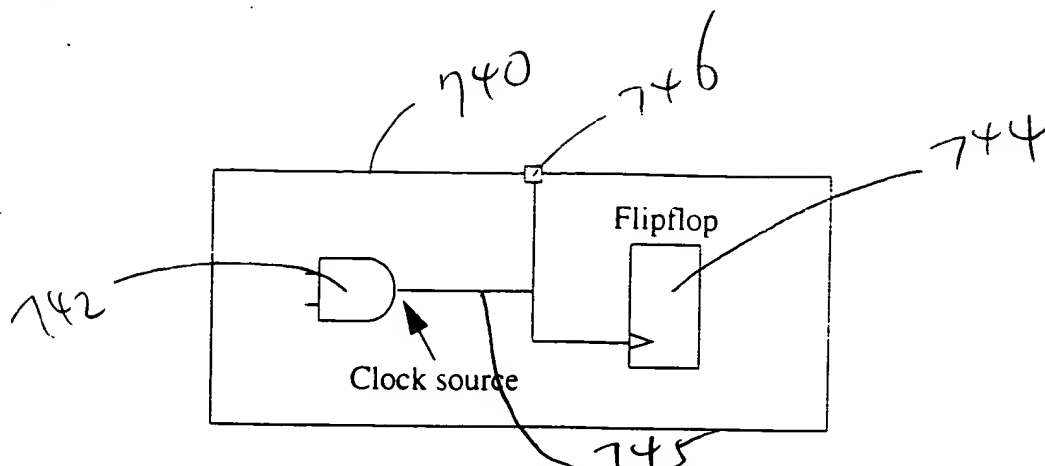


FIGURE 41A Clock source retrieved through using a connected port.

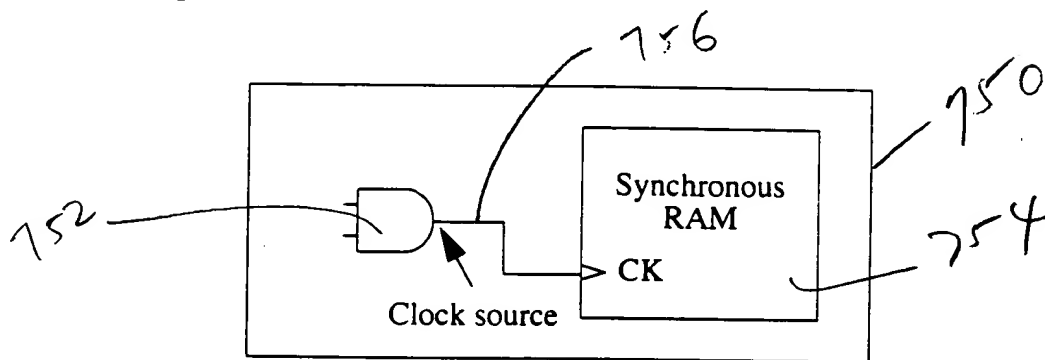


FIGURE 41B Clock retrieved through using a connected clock input pin on a RAM.

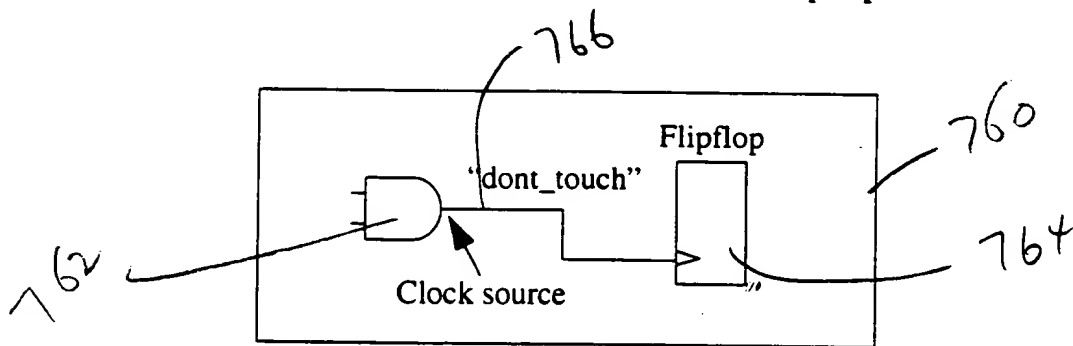


FIGURE 41C Clock source retrieved through using the connected net.

• : Retrieving names of new source pins.

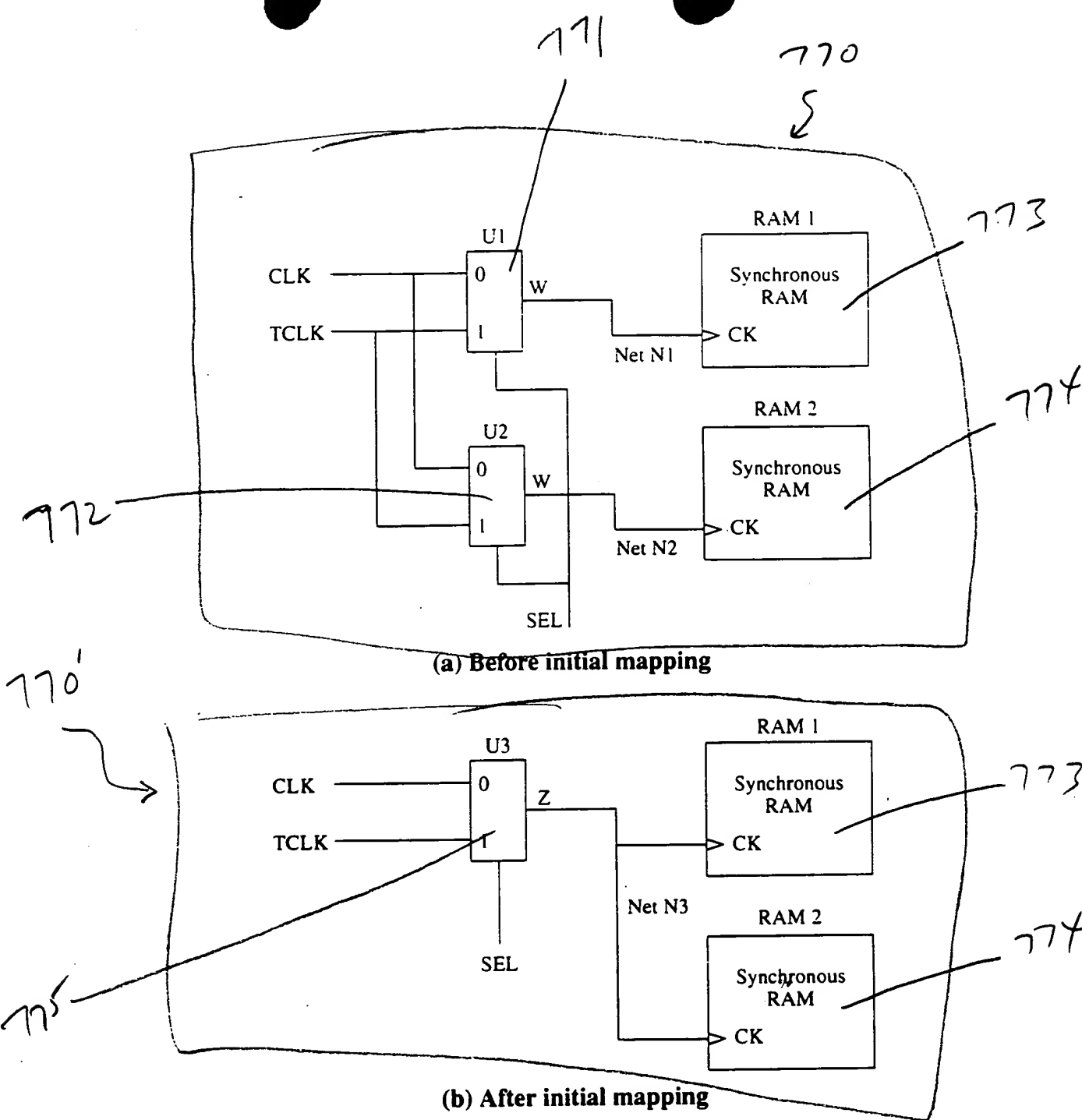


FIGURE 42 : Example of internal clocks altered through initial mapping.

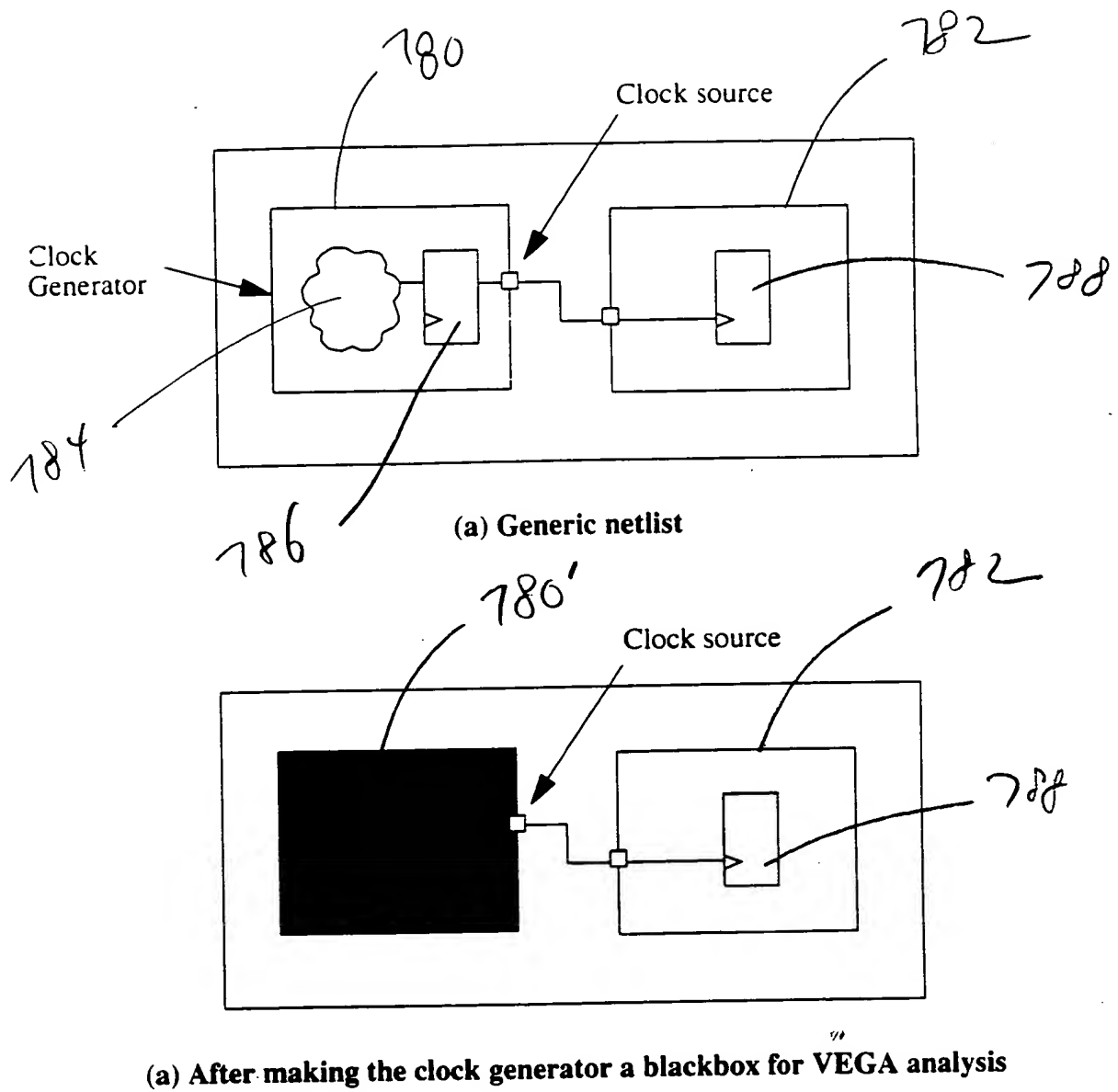


FIGURE 43: Handling clock generators with a "backbox_design" directive.

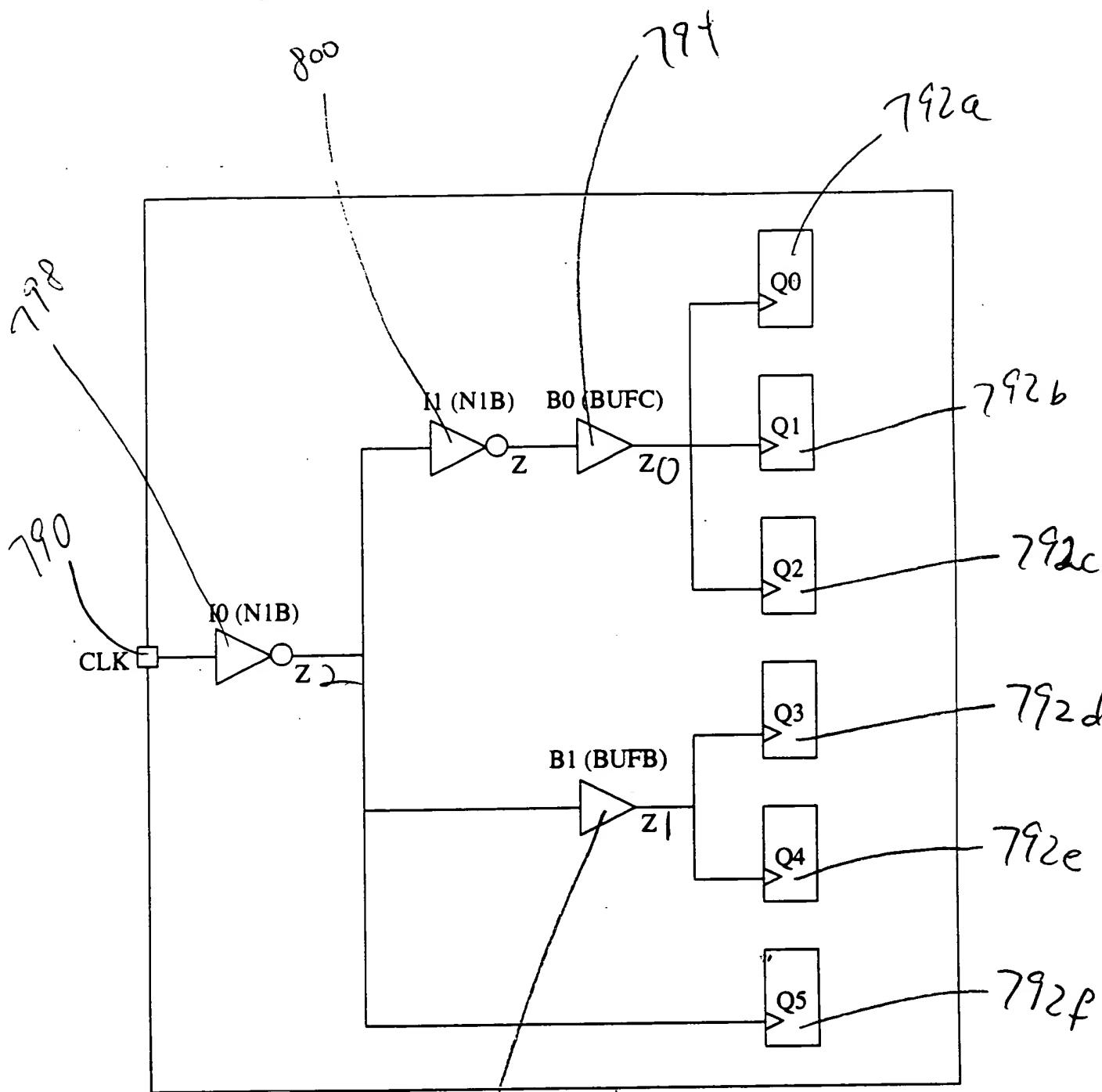


FIGURE 44 : Example of buffering tree used for clock distribution.

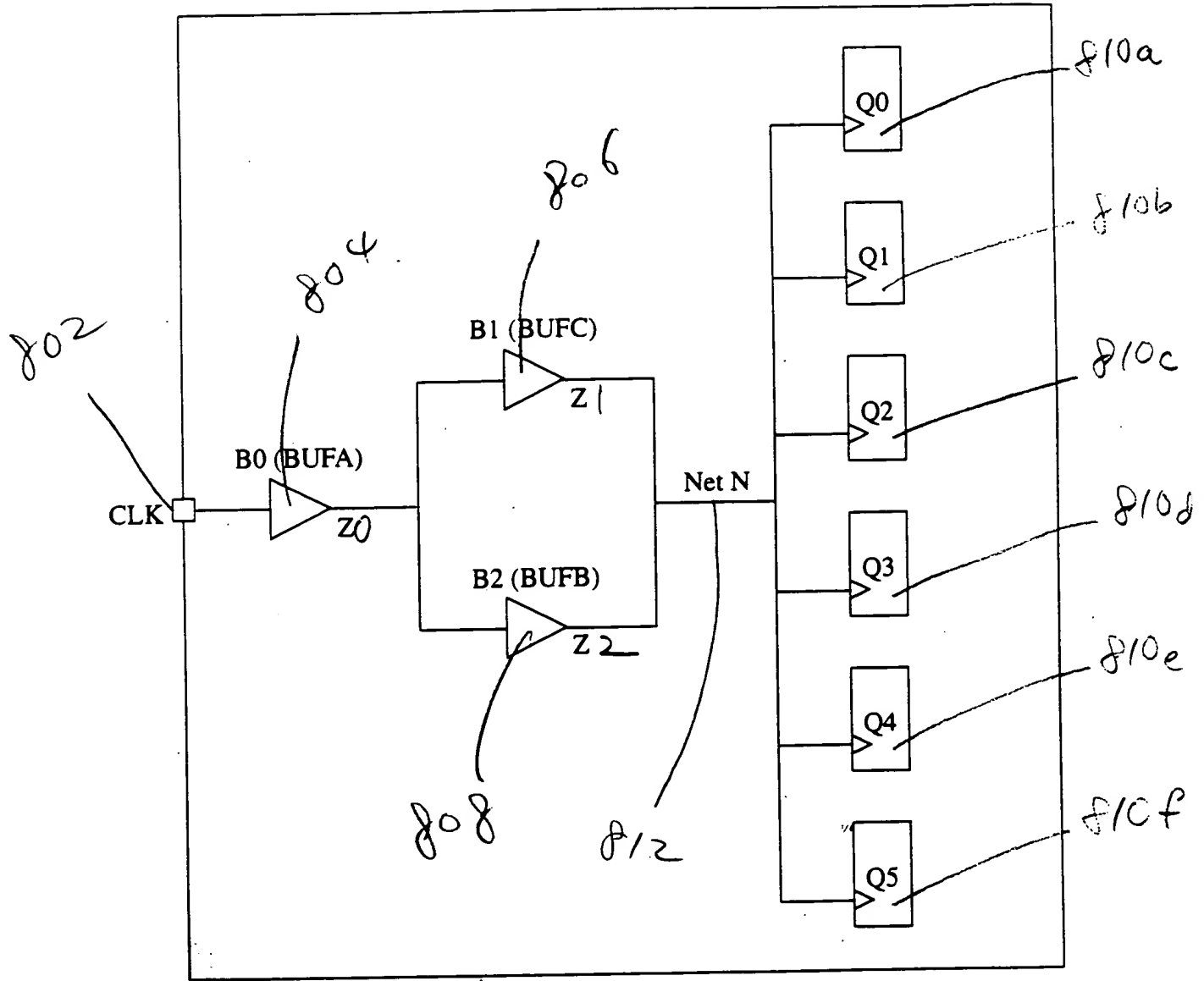


FIGURE 45 : Example of parallel buffers.

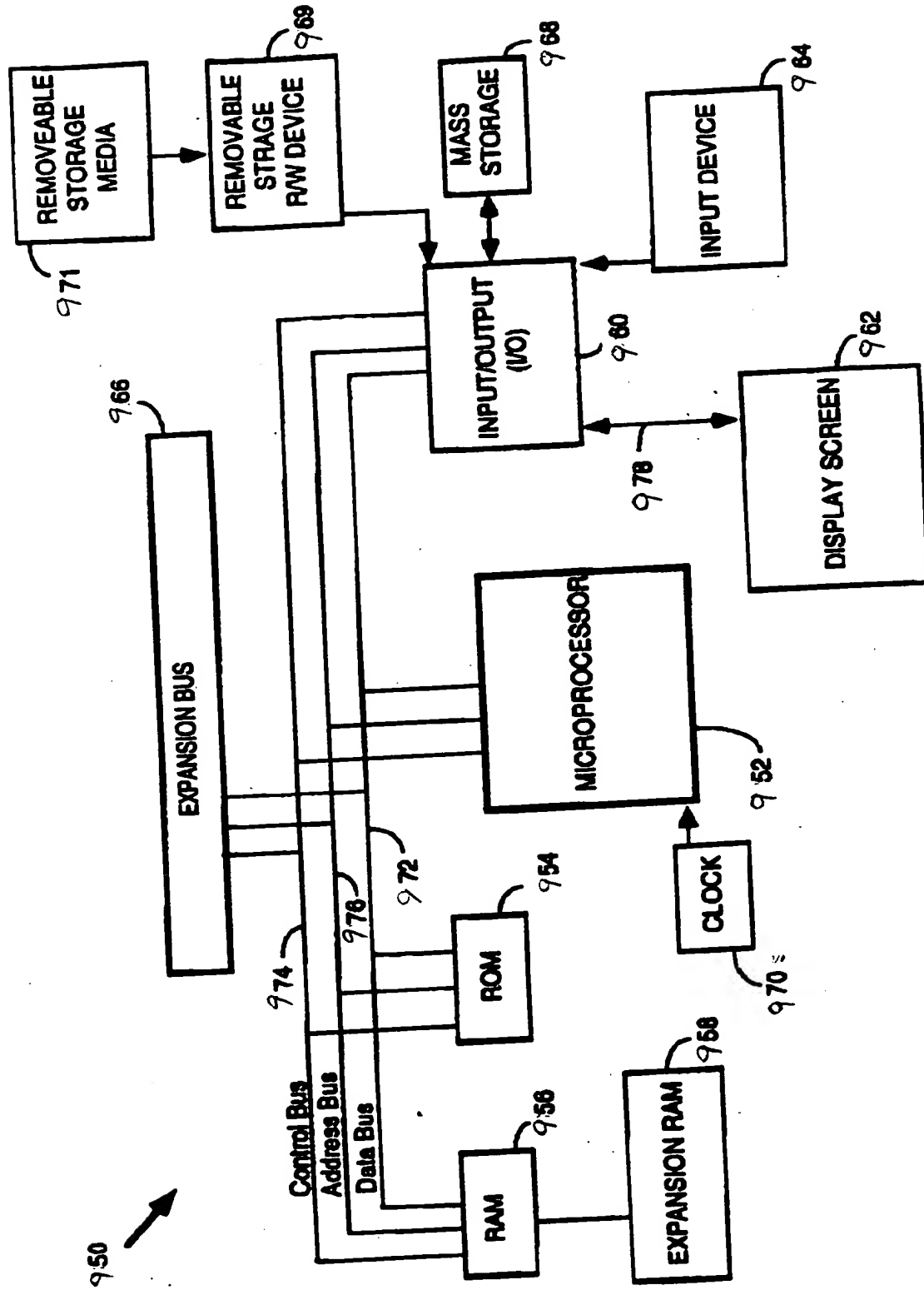


Fig 46

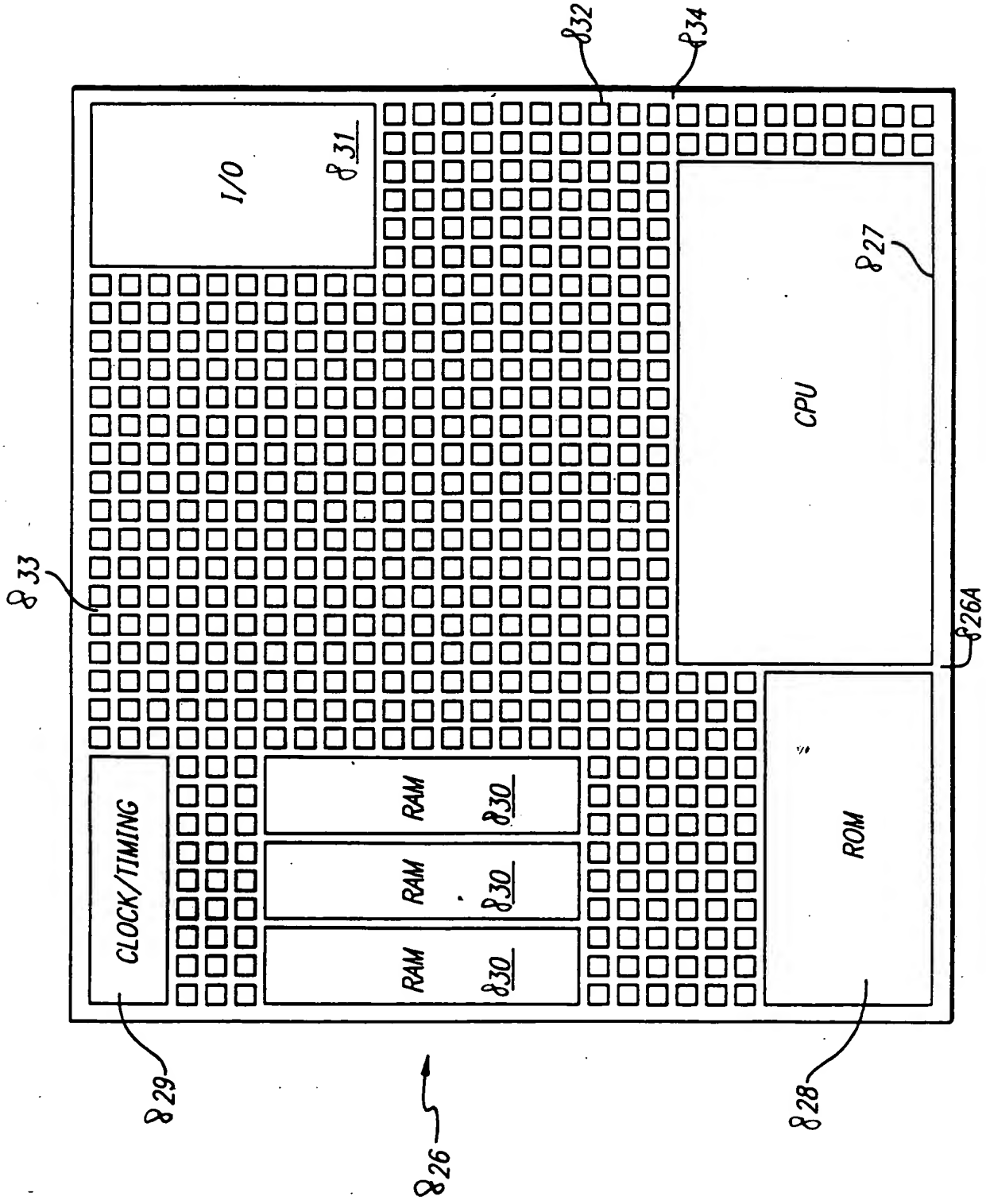


FIG. 47